AKD7755-B

AK7755 Evaluation Board Rev.2

1. General Description

The AKD7755-B is an evaluation board for the AK7755; a mono ADC, a stereo audio CODEC, MIC pre-amplifier, a line-out amplifier and a highly integrated digital signal processor with built-in digital audio interface. This board is composed of a main board and a sub board. It is possible to control the setting of this board via USB port. This board has digital interface, enabling interfacing to digital audio systems via optical connector and SMUX-PORT.

■ Ordering Guide

AKD7755-B --- Evaluation board for AK7755
(Control software is included in this package.)

2. Function

- ☐ **Write/Read RAM: Access to PRAM, CRAM, OFRREG and Registers**
- ☐ **Equipped with two digital audio interface**
  - **Optical Input / Output**
  - **10-pin header for external interfaces**
- ☐ **USB port for board control**

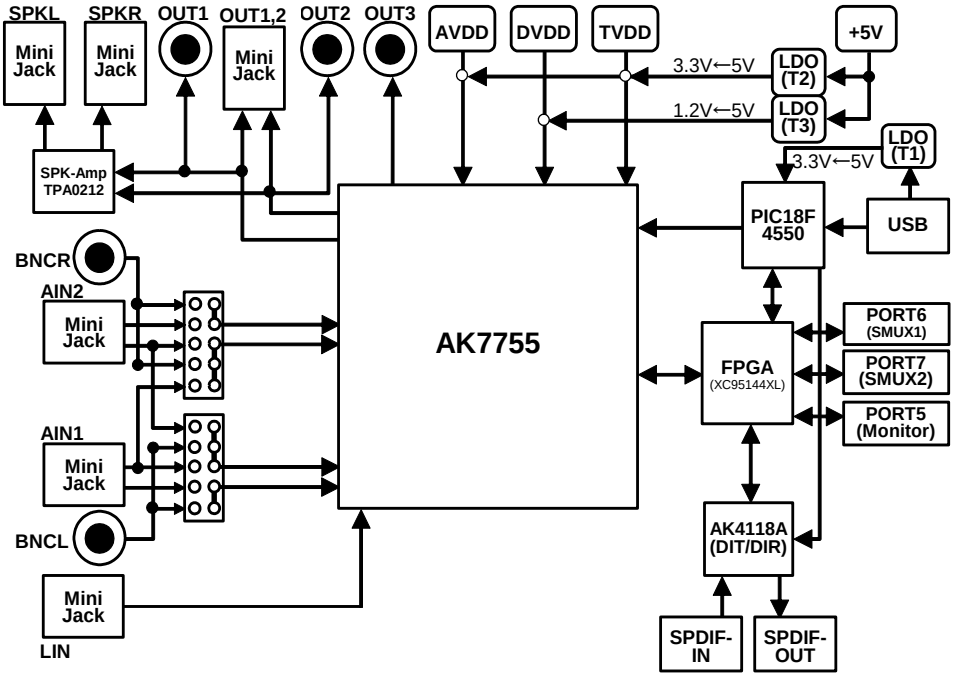


Figure 1. AKD7755-B Block Diagram (Note 1)

Note 1. AK4118A has built-in DIR, DIT and the X'tal oscillator.

3. Table of Contents

4. Evaluation Board

■ Board Diagram

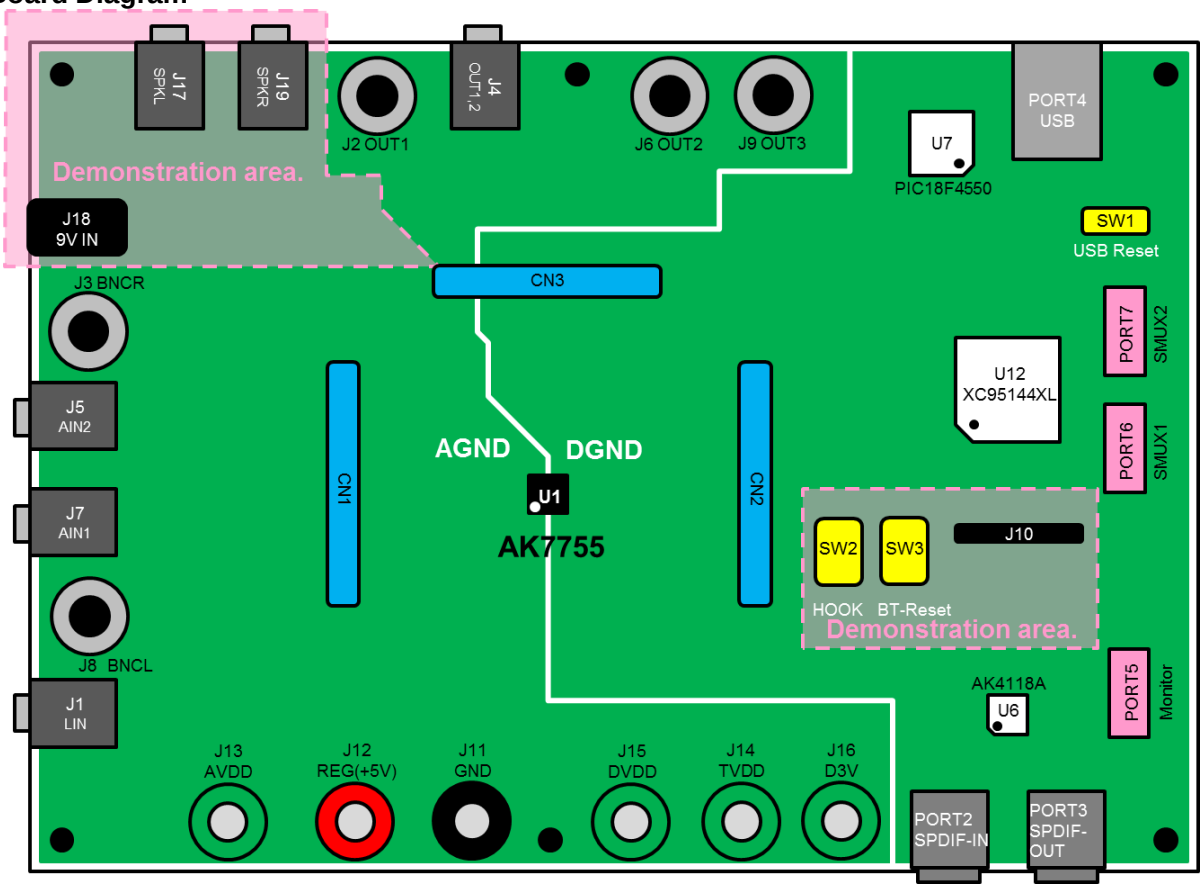


Figure 2. AKD7755-B Board Diagram

■ Description

(1)Analog Input / Output connector

BNCL (J8), BNCR (J3)	: RCA connector for analog single-ended input.
LIN (J1)	: Mini jack for analog single-ended input.
AIN1 (J7), AIN2 (J5)	: Mini jack for analog single-ended / differential input. Refer to the "Set up the analog input".
OUT1 (J2), OUT2 (J6), OUT3 (J9)	: RCA connector for analog single-ended output.
OUT1, 2 (J4)	: Mini jack for analog single-ended output.

(2)AK4118A (U6)

AK4118A has Digital Audio I/F Transceiver.
When evaluating board, Using SPDIF signals with AK4118A.

(3)SPDIF-IN (PORT2) / SPDIF-OUT (PORT3)

SPDIF-IN: Optical input connector. It supports sampling frequencies from 32 kHz to 96 kHz for input.
SPDIF-OUT: Optical output connector. It supports sampling frequencies from 32 kHz to 96 kHz for output.

(4)REG(+5V) / GND / AVDD / TVDD / DVDD / D3V (Power supply)

Refer to the "■ Set up the Power Supply Lines".

(5) PIC18F4550 (U7)
USB control chip.
Control of the AK7755, XC95144XL and AK4118A can be set by a PC via USB port.

(6) USB Reset (SW1)
Push type button.
It is used to initialize the PICIF4550. When connecting the board to PC, it is required to push down the button for initialization.

(7) XC95144XL (U12 / Xilinx)
XC95144XL used for digital signal path control.
It is possible to run a variety of tests by way of controlling the data path via control software.

(8) SMUX PORT (PORT6, PORT7)
10 pin header for connecting with external interface.
Equipped with the two ports, enabling to connect external digital audio systems.

Pin	I/O	Function	pin	I/O	Function
1	I/O	MCLK	2	P	GND
3	I/O	BICK	4	P	GND
5	I/O	LRCK	6	P	GND
7	I/O	SDIN	8	P	GND
9	O	SDOUT	10	P	GND

Table 1. Pin Assignment of SMUX PORT

(9) Monitor PORT (PORT5)
10 pin header for connecting with monitor board.

(10) Demonstration area (Dotted line area of the pink)
It is not used in the normal evaluation.
Nothing should be connected to this area.

5. Operation Sequence

■ Set up the Power Supply Lines

(1)Set up the except for DVDD power supply lines.

(1-1) In case of using the regulator at the all power supply lines. < Default >

Set up the jumper pins.

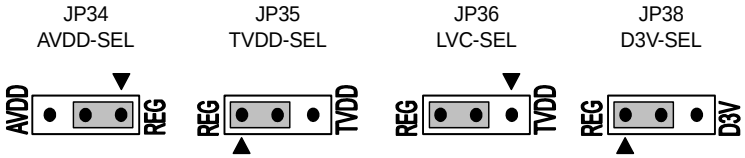


Figure 3. Setting of jumper pins when using the regulator at the all power supply lines.

Set up the power supply lines.

Name	Color	Voltage	Breakdown	Remarks
REG (+5V)	Red	+5V	For regulator	Must be connected.
AVDD	Green	Open	AVDD of AK7755	Must be “open”.
TVDD	Green	Open	TVDD of AK7755	Must be “open”.
D3V	Green	Open	Digital Logic	Must be “open”.
GND	Black	0V	Ground	Must be connected.

Table 2. Set up of power supply lines (Note 2).

(1-2) In case of using the power supply connector.

Set up the jumper pins.

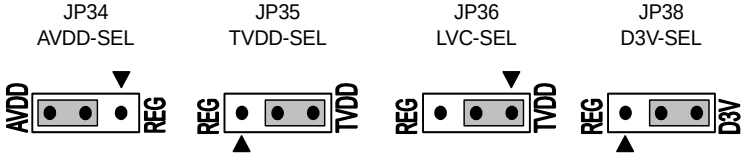


Figure 4. Setting of jumper pins when using the power supply connector.

Set up the power supply lines.

Name	Color	Voltage	Breakdown	Remarks
REG (+5V)	Red	+5V	For regulator	Must be “open”.
AVDD	Green	+3.0V - +3.6V [typ :+3.3V]	AVDD of AK7755	Must be connected.
TVDD	Green	+1.7V - +3.6V [typ :+3.3V]	TVDD of AK7755	Must be connected.
D3V	Green	+3.0V - +3.6V [typ :+3.3V]	Digital Logic	Must be connected.
GND	Black	0V	Ground	Must be connected.

Table 3. Set up of power supply lines (Note 2, Note 3).

Note 2. TVDD and LVC must be same voltage level.
Note 3. Each supply line should be distributed from the power supply unit.

(2)Set up of DVDD power supply lines.

(2-1) In case of using the Internal LDO at the DVDD power supply line. (LDOE pin = "H"). < Default >

Set up the jumper pins.

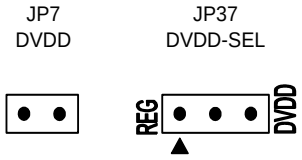


Figure 5. Setting of jumper pins when using the Internal LDO at the DVDD power supply line.

(2-2) In case of using the external power supply at the DVDD power supply line. (LDOE pin = "L")

(2-2-1) In case of using regulator.

Set up the jumper pins.

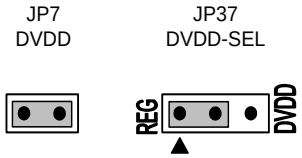


Figure 6. Setting of jumper pins when using regulator.

Set up the power supply lines.

Name	Color	Voltage	Breakdown	Remarks
DVDD	Green	Open	DVDD of AK7755	Must be "open".

Table 4. Set up of DVDD power supply lines when using regulator (Note 4).

Note 4. In case of using the external regulator at the DVDD power supply line, should be supplied "+5V" at the J12 (REG (+5V)) connector.

(2-2-2) In case of using the power supply connector.

Set up the jumper pins.

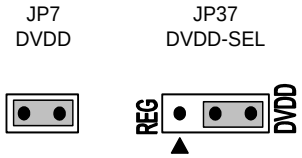


Figure 7. Setting of jumper pins when using the power supply connector.

Set up the power supply lines.

Name	Color	Voltage	Breakdown	Remarks
DVDD	Green	+1.1V - +1.3V [typ :+1.2V]	DVDD of AK7755	Must be connected.

Table 5. Set up of DVDD power supply lines when using the power supply connector (Note 3).

■ Evaluation Mode

XC95144XL and AK4118A are controlled by the control software. The software operation sequence is referring to the “Control Soft Manual”.

(1)Set up the analog input

When using the monaural ADC, J1 (LIN) is used.
When using the stereo ADC, the jumper settings will depend on the type of analog input signal and cable used.

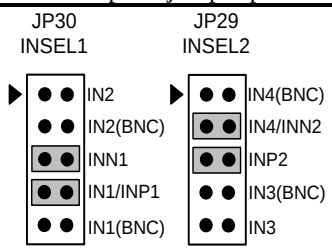
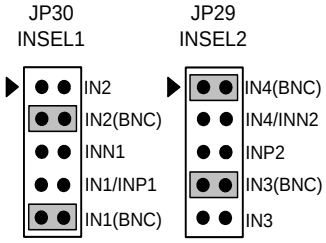
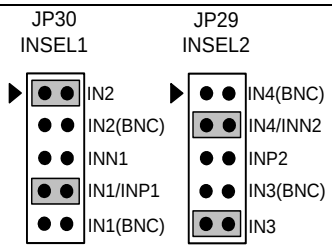
Input Signal	Use cable	Connection	Set up the jumper pins
Differential < Default >	Mini jack	J7 (AIN1) J5 (AIN2)	
Single-ended	RCA	J8 (BNCL) J3 (BNCR)	
Single-ended	Mini jack	J7 (AIN1) J5 (AIN2)	

Table 6. Set up of stereo ADC evaluation.

(2) A/D, D/A and DSP evaluation using the SMUX1 and SMUX2 PORT.

(2-1) Evaluation of CKM Mode = 0 / 1.

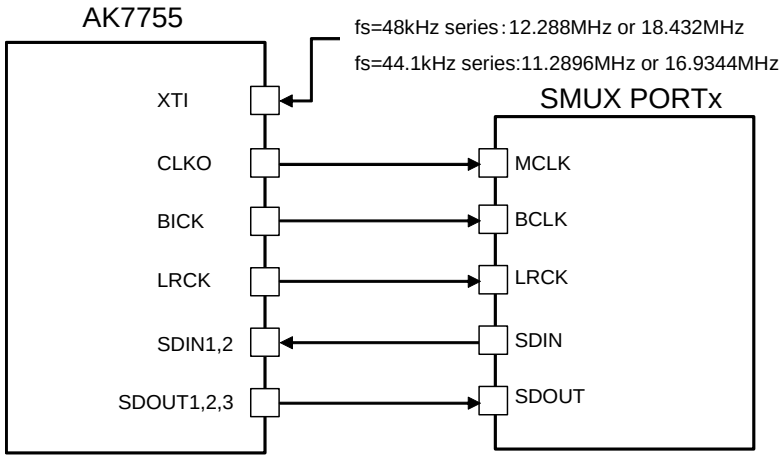


Figure 8. CKM Mode = 0 / 1

X1 and PORT6 (SMUX1) or PORT7 (SMUX2) are used. XTI is supplied from the X1 (X'tal). CLKO, BICK, LRCK and SDOUT1, 2, 3 of the AK7755 are output to the PORT6 (SMUX1) or PORT7 (SMUX2), and SDIN1, 2 are supplied from PORT6 (SMUX1) or PORT7 (SMUX2).

Set up the jumper pins.

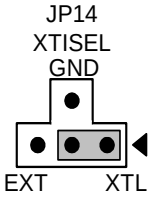


Figure 9. Setting of jumper pins

(2-2) Evaluation of CKM Mode = 2 / 3.

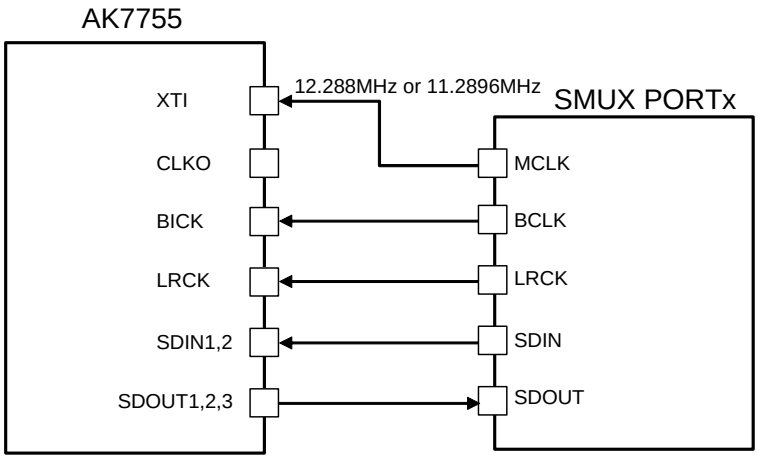


Figure 10. CKM Mode = 2 / 3

PORT6 (SMUX1) or PORT7 (SMUX2) are used.
XTI (Note 5), BICK, LRCK, SDIN1, 2 are supplied from PORT6 (SMUX1) or PORT7 (SMUX2), and SDOUT1, 2, 3 of AK7755 are output to the PORT6 (SMUX1) or PORT7 (SMUX2).

Set up the jumper pins.

CKM Mode = 2 CKM Mode = 3

Figure 11. Setting of jumper pins

Note 5. XTI pin is used only CKM Mode = 2 setting. In addition, should be connected to GND to XTI pin is CKM Mode = 3 setting.

(2-3) Evaluation of CKM Mode = 5.

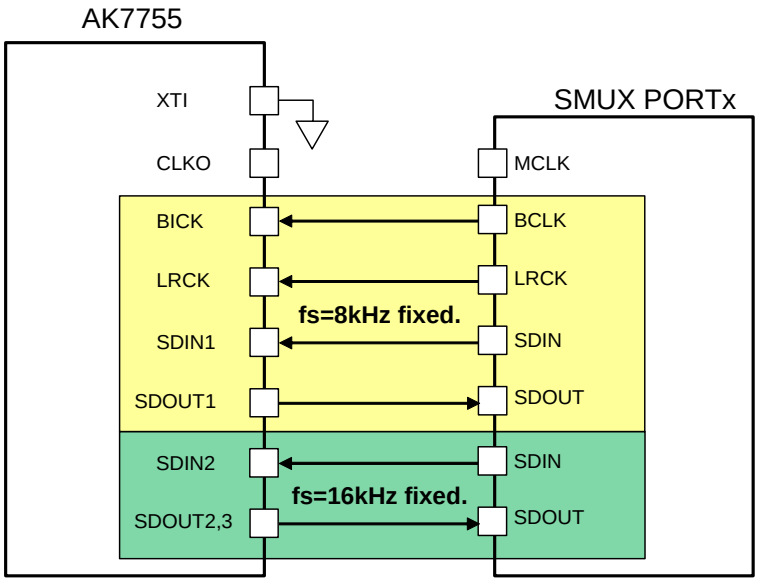


Figure 12. CKM Mode = 5

PORT6 (SMUX1) or PORT7 (SMUX2) is used.
BICK, LRCK, SDIN1, 2 are supplied from PORT6 (SMUX1) or PORT7 (SMUX2), and SDOUT1, 2, 3 of AK7755 is output to the PORT6 (SMUX1) or PORT7 (SMUX2).
At this time, SDIN1, SDOUT1, BICK, LRCK is “fs = 8 kHz” fixed, and SDIN2, SDOUT2, 3 is “fs = 16 kHz” fixed.

Set up the jumper pins.

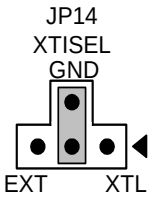


Figure 13. Setting of jumper pins

(3) A/D and D/A evaluation using the AK4118A.

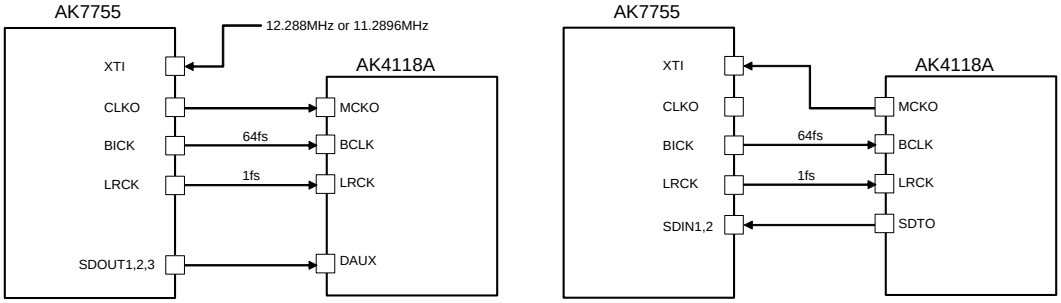
In case of using the AK4118A when evaluating the AK7755, check the following settings.

Audio I/F Format:	Both the AK7755 and AK4118A's audio interface formats must be matched. Refer to the datasheet for AK7755's audio interface format, and AK4118A's audio interface format.
MCLK:	MCLK is supports only 128fs and 256fs (Note 6).
BICK:	BICK is support only 64fs (Note 6).
LRCK:	Sampling frequency is supports 32 kHz more than 96 kHz (Note 6).

Note 6. When evaluating in a condition except above, please use other mode.

(3-1) Evaluation of CKM Mode = 0 < Default >.

AK4118A should be set to "Slave Mode".



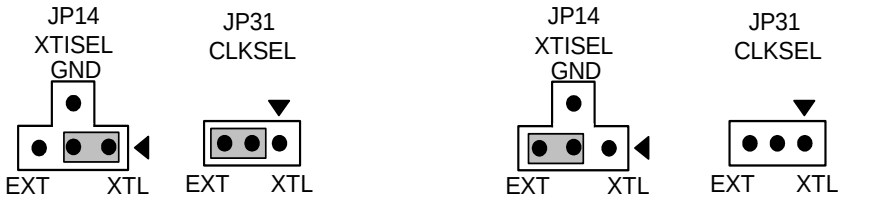
Evaluation of A/D Evaluation of D/A

Figure 14. CKM Mode = 0.

When evaluating of A/D using DIT function of AK4118A, X1 and PORT3 (SPDIF-OUT) are used.
XTI is supplied from X1 (X'tal), and CLKO, BICK, LRCK and SDOUT1, 2, 3 is output to the AK4118A.

When evaluating of D/A using DIR function of AK4118A, PORT2 (SPDIF-IN) is used.
XTI and SDIN1, 2 are supplied from AK4118A, and BICK and LRCK is output to the AK4118A.

Set up the jumper pins.



Evaluation of A/D Evaluation of D/A < Default >

Figure 15. Set up the jumper pins.

(3-2) Evaluation of CKM Mode = 2 / 3.

AK4118A should be set to “Master Mode”.

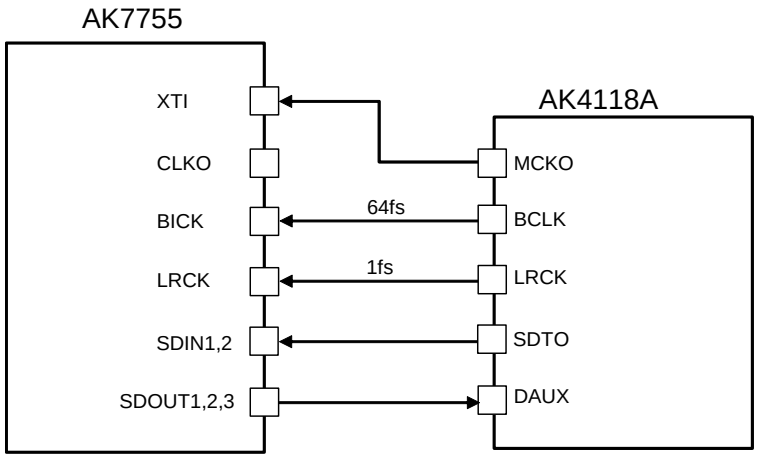


Figure 16. CKM Mode = 2 / 3.

When evaluating of A/D using DIT function of AK4118A, X2 and PORT3 (SPDIF-OUT) are used.
XTI, BICK, LRCK are supplied from PORT3 (SPDIF-OUT), and SDOUT1, 2, 3 is output to the AK4118A.

When evaluating of D/A using DIR function of AK4118A, PORT2 (SPDIF-IN) is used.
XTI, BICK, LRCK and SDIN1, 2 are supplied from AK4118A.

Set up the jumper pins.

Evaluation of A/D Evaluation of D/A

Figure 17. Set up the jumper pins.

■ Jumper pins Setting

(1) Setting of other jumper pins.

(1-1) Main Board.

[JP33] (GND): Analog ground and digital ground.
OPEN : None connect to GND.
SHORT : Connect to GND. < Default >

(1-2) Sub Board.

[JP1] (IN1MP): The selection of MIC-power of IN1 pin.
OPEN : MIC-power is not supplied. < Default >
SHORT : MIC-power is supplied.

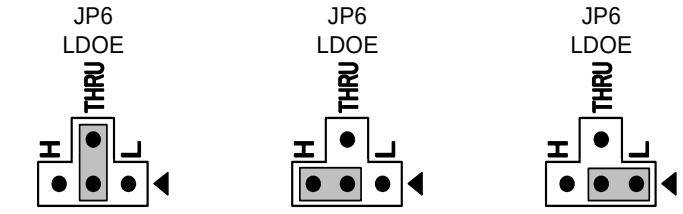
[JP2] (IN3MP): The selection of MIC-power of IN3 pin.
OPEN : MIC-power is not supplied. < Default >
SHORT : MIC-power is supplied.

[JP3] (IN2MP): The selection of MIC-power of IN2 pin.
OPEN : MIC-power is not supplied. < Default >
MP : MIC-power is supplied.
GND : Connect to GND.

[JP4] (IN4MP): The selection of MIC-power of IN4 pin.
OPEN : MIC-power is not supplied. < Default >
MP : MIC-power is supplied.
GND : Connect to GND.

[JP5] (LINMP): The selection of MIC-power of LIN pin.
OPEN : MIC-power is not supplied. < Default >
SHORT : MIC-power is supplied.

[JP6] (LDOE): The selection of connection of LDOE pin.
THRU : When using controlling from main board. < Default >
H : LDOE pin is fixed to “H”.
L : LDOE pin is fixed to “L”.



Select to “THRU” Select to “H” Select to “L”

Figure 18. Set up the jumper pins.

[JP8] (HB5): The selection of the standalone operation of sub board.
OPEN : When using along with the main board. < Default >
SHORT : When using the standalone operation of sub board.

[JP9] (HB4): The selection of the standalone operation of sub board.
OPEN : When using along with the main board. < Default >
SHORT : When using the standalone operation of sub board.

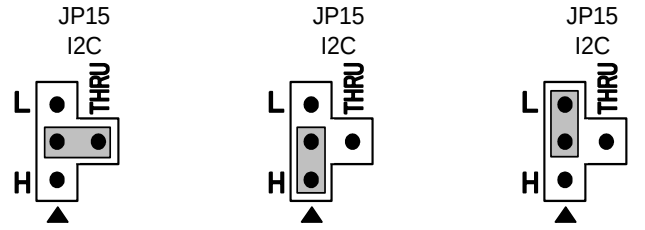
[JP10] (CSN/CAD): The selection of input signal to CSN/CAD pin.
OPEN : Not connect.
SHORT : Connect. < Default >

[JP11] (SCLK/SCL): The selection of input signal to SCLK/SCL pin.
OPEN : Not connect.
SHORT : Connect. < Default >

[JP12] (SO/SDA): The selection of input signal to SO/SDA pin.
OPEN : Not connect.
SHORT : Connect. < Default >

[JP13] (HB1): The selection of the standalone operation of sub board.
w/ Main : When using along with the main board. < Default >
w/o Main : When using the standalone operation of sub board.

[JP15] (I2C): The selection of connection of I2C pin.
THRU : When using controlling from main board. < Default >
H : I2C pin is fixed to “H”.
L : I2C pin is fixed to “L”.



Select to “THRU” Select to “H” Select to “L”

Figure 19. Set up the jumper pins.

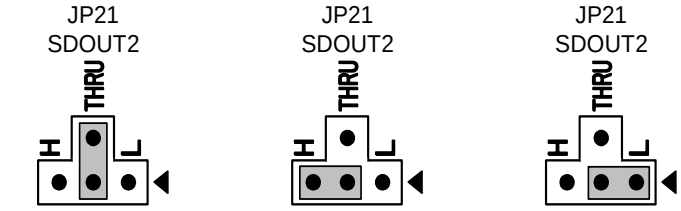
[JP16] (SDIN1): External digital signal input pin header.
In case of using digital signal from externally, R40 should be open.

[JP17] (LRCK): External digital signal input / output pin header.
In case of using digital signal from externally, R43 should be open.

[JP18] (BICK): External digital signal input / output pin header.
In case of using digital signal from externally, R45 should be open.

[JP19] (CLKO): External digital signal output pin header.
In case of using digital signal from externally, R47 should be open.

[JP21] (SDOUT2): The selection of connection of SDOUT2 /JX3/MAT0 pin.
THRU : When using controlling from main board. < Default >
H : JX3 or MAT0 pin is fixed to “H”.
L : JX3 or MAT0 pin is fixed to “L”.



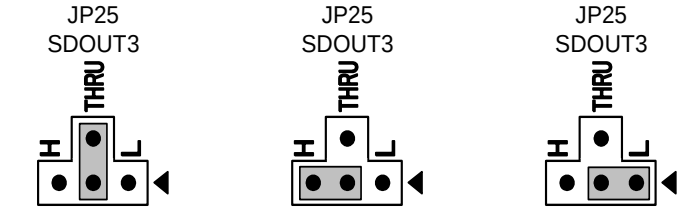
Select to “THRU” Select to “H” Select to “L”
Figure 20. Set up the jumper pins.

[JP22] (HB2): The selection of the standalone operation of sub board.
OPEN : When using along with the main board. < Default >
SHORT : When using the standalone operation of sub board.

[JP23] (HB3): The selection of the standalone operation of sub board.
OPEN : When using along with the main board. < Default >
SHORT : When using the standalone operation of sub board.

[JP24] (SDIN2): External digital signal input pin header.
In case of using digital signal from externally, R38 should be open.

[JP25] (SDOUT3): The selection of connection of SDOUT3 /JX2/MAT1 pin.
THRU : When using controlling from main board. < Default >
H : JX2 or MAT1 pin is fixed to “H”.
L : JX2 or MAT1 pin is fixed to “L”.

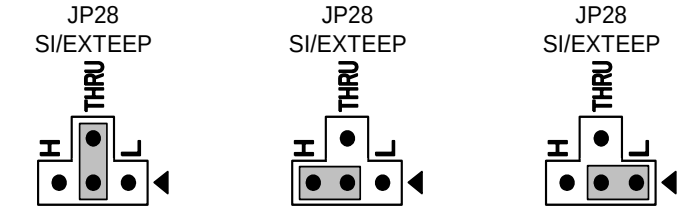


Select to “THRU” Select to “H” Select to “L”
Figure 21. Set up the jumper pins.

[JP26] (SDOUT1): External digital signal output pin header.
In case of using digital signal from externally, R52 should be open.

[JP27] (HB6): The selection of the standalone operation of sub board.
OPEN : When using along with the main board. < Default >
SHORT : When using the standalone operation of sub board.

[JP28] (SI/EXTEEP): The selection of connection of SI/EXTEEP pin.
THRU : When using controlling from main board. < Default >
H : EXTEEP pin is fixed to “H”.
L : EXTEEP pin is fixed to “L”.



Select to “THRU” Select to “H” Select to “L”
Figure 22. Set up the jumper pins.

(2) Function of the SW.

[SW1] (USB Reset): Initialize switch of PIC18F4550.
PUSH : It is used to initialize the PIC18F4550.
When connecting the board to PC, it is required to push down the button for initialization.
RELEASE : It is not used to initialize the PIC18F4550. < Default >

[SW2] (HOOK): Not to use.

[SW3] (BT-Reset): Not to use.

■ Indication for LED

[D1]: When power of PIC18F4550 is supplied, LED is lighted to red.

[D2]: Not to use.

[D3]: The status of AK7755’s STO/RDY pin is displayed. “L” -> Light on; “H” -> Light off.

■ Board Control

The AKD7755-B can be controlled via a USB port with a PC. Connect PORT4 (USB) connector to a PC with USB cable. The control software is included in the AKD7755-B package. Refer to the “Control Soft Manual” paragraph for operational sequence of the control software.

6. Control Soft Manual

■ Evaluation Board and Control Software Setting

(1) Connect the evaluation board and PC with a USB cable (Note 7).

Note 7. The USB control is recognized as HID (Human Interface Device) on the PC.
This connection can be checked in the device manager.

(2) Access the CD-ROM (labeled "AKD7755-B Evaluation Kit") and execute "AK7755-BHF.exe" (Note 8).

(3) When using Bluetooth, connect a mobile phone to Bluetooth Module.
Refer to the evaluation flow of above-mentioned in Bluetooth mode.

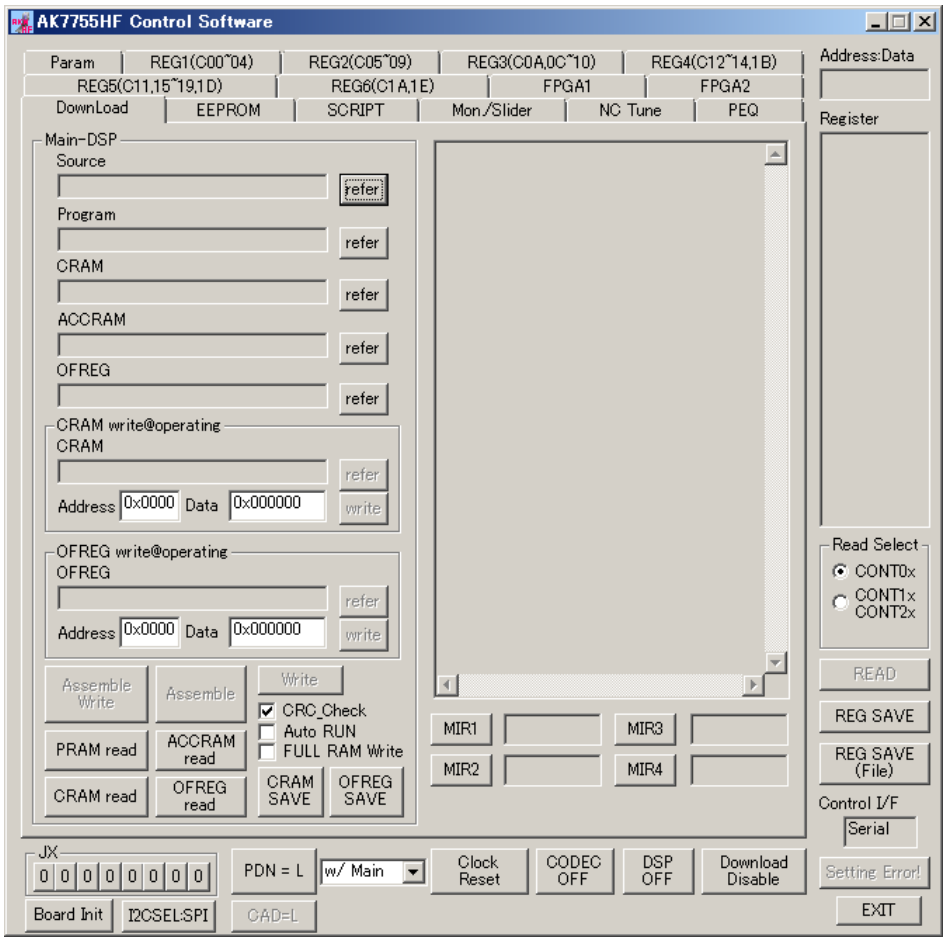


Figure 23. Startup Screen

Note 8. The software must run again when disconnecting the USB cable which connects PC and the evaluation board.

■ Operation Overview

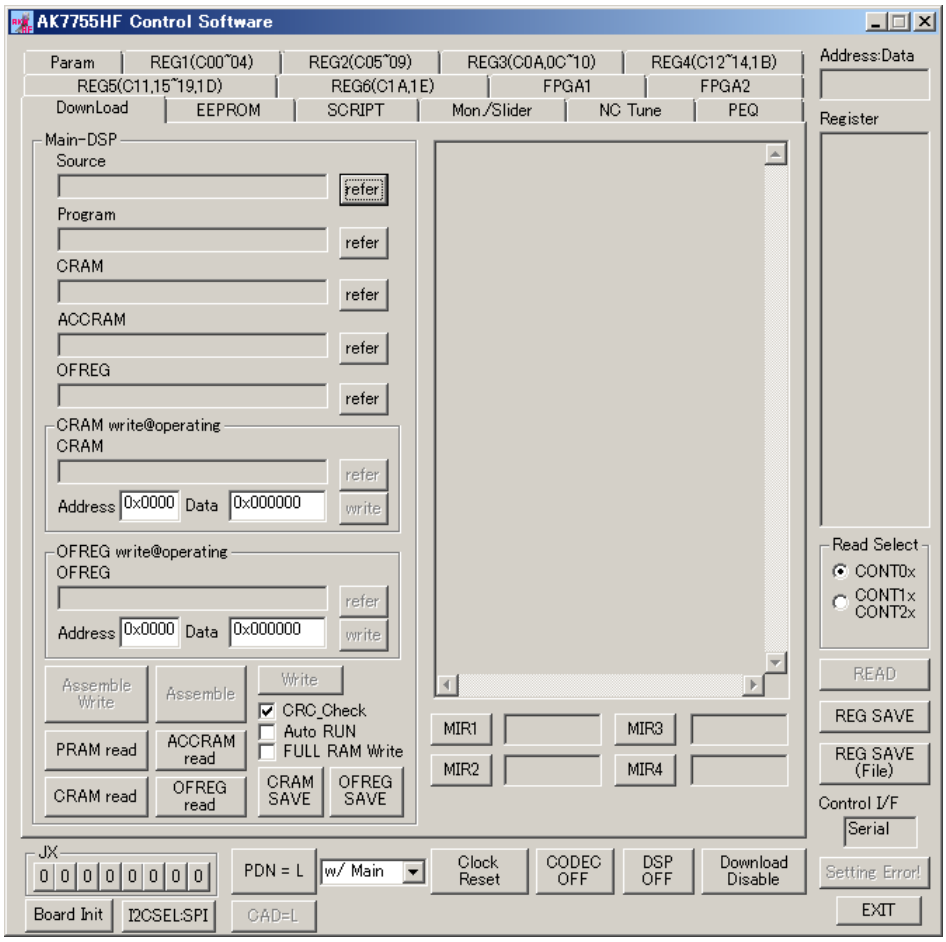


Figure 24. Window of Control Soft

Function and Register map are controlled by this control software. These controls may be selected by the upper tabs.

Frequently used Buttons, such as the register initializing button “READ”, are located outside of the switching tab window. The interface (SPI or I2C) which software recognized is displayed on the “Control I/F” column. When AKD7755-B is not connected with PC, “Error!” is displayed on the column.

[Board Init]:	Reset the evaluation board, and the register values setup on the control software are written again. When PDN pin = H, Hardware reset (PDN pin = "L" ->"H") is executed before register writing.
[I2CSEL: SPI/I2C]:	Selection of control I/F. This can be changed at PDN = L.
[CAD = L/H]:	When mode is I2C, CAD pin can be set. This can be changed at the PDN = “L”. The CAD button is fixed to “L” if MATSEL function is enabled on the “EEPROM” tab.
[PDN = L/H]:	Control of the PDN pin of AK7755. (L: Power down and initialize the AK7755) When PDN = L, the register setup on software is also set to default value.
[w/ Main, w/o Main]:	The selection of the standalone operation of sub board. When using along with the main board, select to the "w/ Main". And when using the standalone operation of sub board, select to the "w/o Main".

[Clock Reset/Enable]: Selection of RESET/Enable of Clock. (Control of CKRESETN bit)
RESET : CKRESETN bit = 0
Enable : CKRESETN bit = 1
When using CODEC/DSP, it is necessary to set this to “Enable”.

[CODEC OFF/ON]: Control of CODEC’s ON/OFF. (Control of CRESET bit)
OFF : CRESET bit = 0
ON : CRESET bit = 1

[DSP OFF/ON]: Control of DSP’s ON/OFF. (Control of DSPRESETN bit)
OFF : DSPRESETN bit = 0
ON : DSPRESETN bit = 1

[Download Disable/Enable]: Control of Disable/Enable of DSP code download under a main clock stop or clock reset. (Control of DLRDY bit) This should be set to “Disable” after finishing download.
Disable : DLRDY bit = 0
Enable : DLRDY bit = 1

[JX]: JX Code Setting.

[READ]: Reads out register values and shows them on the “Register” column (Note 9).
CONT0x : Read out of CONT00 - CONT0A, CONT0C - CONT0F.
CONT1x, CONT2x : Read out of CONT10 - CONT1B, CONT1D - CONT1E, CONT26, CONT2A

[REG SAVE]: Register setting is saved. (A file name is “_Reg_setting.txt”.)

[REG SAVE(File)]: Register setting is saved. (A file name can be choices.)
Since a file name setting dialog opens after pushing this button, please set up the file name to save.

[Setting Error!]: [Setting Error] dialog opens and it displays the information on some invalid setup.
When some invalid setup is carried out on GUI, this button becomes effective.

Note 9. When PDN = H, it will enable to access for register of AK7755.

■ Tab Functions

(1) “DownLoad” Dialog

There are three code areas in the AK7755 as below.
Setup of a register is a “REGx” tab. And “Download” tab can download program code and coefficient values to RAM.

Code Area	Alias	Function
Control Register	CONT	AK7755 operation mode setup
Program RAM	PRAM	RAM for HF program codes
Coefficient RAM	CRAM	Setting parameter used on the HF program

Table 7. AK7755 code area

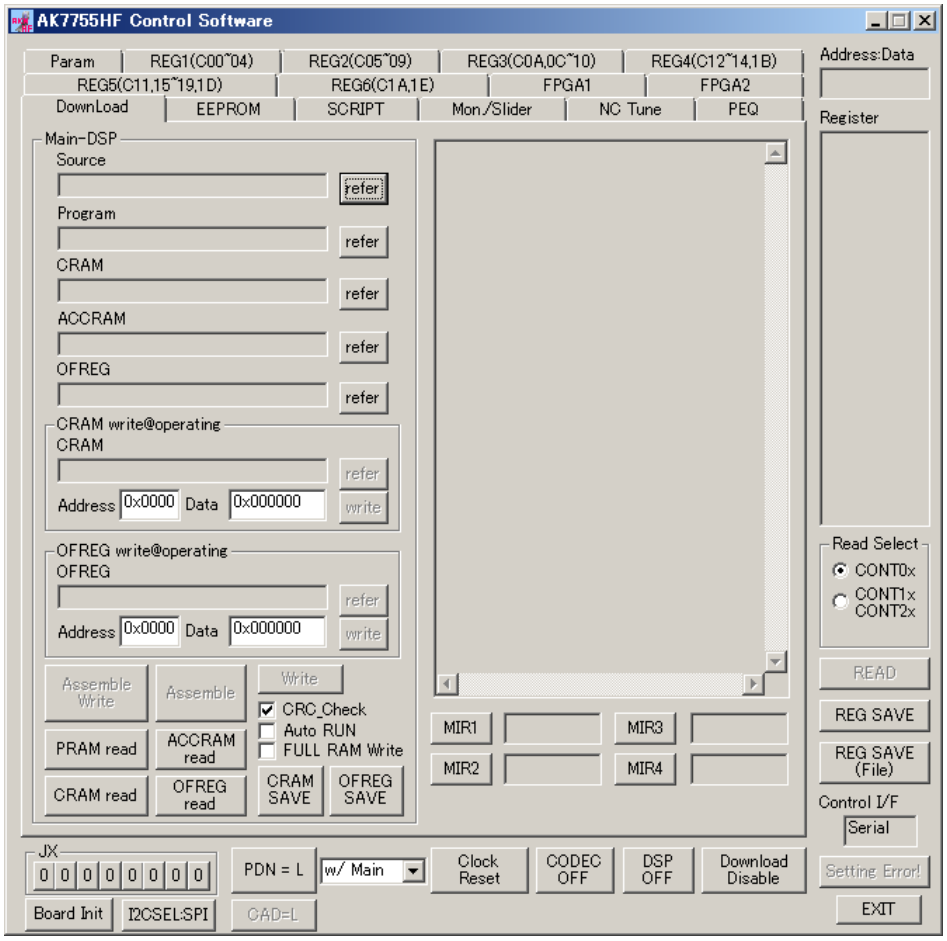


Figure 25. “DownLoad” Dialog

Select a file for Source box, Program box, CRAM box, ACCRAM box or OFREG box by clicking the [refer] button of each box.

Select a file for CRAM/OFRAM box by clicking [refer] button. Then CRAM/OFREG writings during RUN are available. When [write] button clicked, the specified data will be written to the address given by CRAM/OFREG box. When Clock Enable and DSP ON, [refer] and [write] button can be used.

[Assemble]:	Compiles the selected source file, and the output file will be selected to the download program automatically.
[Write]:	Downloads the program file, CRAM file, ACCRAM file and OFREG file to the AK7755.
[Assemble Write]:	Compiles the source file, and then downloads the program file to the AK7755.
[PRAM read]:	Reads the data of PRAM to a temporary file and opens the file.
[CRAM read]:	Reads the data of CRAM to a temporary file and opens the file.
[ACCRAM read]:	Reads the data of ACCRAM to a temporary file and opens the file.
[OFREG read]:	Reads the data of OFREG to a temporary file and opens the file.
[CRAM SAVE]:	Reads the data of CRAM and saves to a file.
[OFREG SAVE]:	Reads the data of OFREG and saves to a file.
[MIR1 - 4]:	Reads the data of register MICR1 - MIR4 when a program is running and displays the result.
[CRC-Check]:	If this box is checked, simple write error check is done by CRC when downloading a file to theAK7755.
[Auto RUN]:	If this box is checked, the AK7755 will be set to run mode automatically after downloading a program. (CKRESETN bit = CRESETN bit = DSPRESETN bit = 1)
[Full RAM Write]:	If this box is checked, all memories of RAM are written. (“0” data are written in the area which is not existed in the download files).

Note 10. When download is executed at clock-reset and download-disable, DLRDY bit is set to 1 before download. When download finished, DLRDY bit is returned to 0.

(2) “EEPROM” Dialog

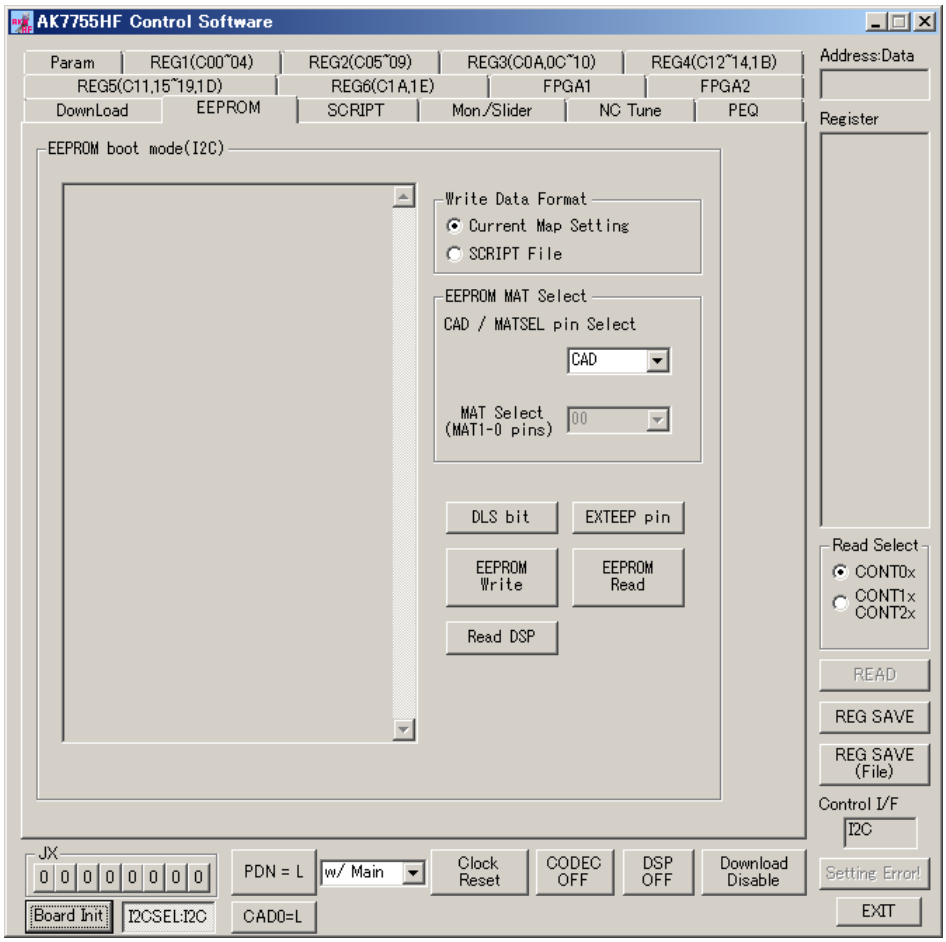


Figure 26. “EEPROM” Dialog

When mode is I2C, AK7755 can download the data of EEPROM that were written by this control soft before.

[Write Data Format]:	As the data written in the EEPROM, the current values on this software, or the data in arbitrary Script files (Note 12) can be chosen.
[CAD / MATSEL pin Select]:	When “MATSEL” is set, the mat select of EEPROM is available.
[MAT Select]:	Selection of EEPROM MAT.
[EEPROM Write]:	Write the data of Register setting, PRAM, CRAM, OFREG to the EEPROM.
[EEPROM Read]:	Read the data of Register setting, PRAM, CRAM, OFREG from the EEPROM.
[DLS bit]:	When “0”->“1”, AK7755 starts download of EEPROM data.
[EXTEEP pin]:	When “L”->“H”, AK7755 starts download of EEPROM data.
[Read DSP]:	Read the register of AK7755 and these read data are reflected in the software.

Note 11. EEPROM function is enable at I2C mode ([I2CSEL: SPI/I2C] = I2C).

Note 12. If the statement of command in the script file do not correspond with the program map for EEPROM of AK7755. Command is same as command of a “Script” tab. However, this does not use except “W”, “LP”, “LC”, “LO”.

[Write sequence to external EEPROM]

1. [I2CSEL] box: Set to “I2C I/F”.
2. When using MAT function,
   [CAD / MATSEL pin Select] (EEPROM tab function): Set to “MATSEL”.
3. [PDN=L/H] button: Set to “PDN = H”.

   When using “Script File”, start from 7.

4. Set register values in “REGx” tab.
5. “Download” tub setting
   5-1. Select a Program file by [refer] button.
   5-2. Select a CRAM file by [refer] button.
   5-3. Select an OFREG file by [refer] button.
   5-4. Write in to RAM with the [Write] button.
6. Setting of control buttons outside of the tab window
   6-1. [Clock Reset/Enable]: Set to “Enable”.
   6-2. [CODEC OFF/ON]: Set to “ON”.
   6-3. [DSP OFF/ON]: Set to “ON”.
7. “EEPROM” tub setting
   7-1. Select Write Data Format (Current Map Setting / SCRIPT File).
   7-2. When using MAT function, set MAT1-0 pins by the [MAT Select] combo box.
   7-3. Write to EEPROM with the [EEPROM Write] button.
   7-4. When using “Script File”, select a file by a dialog box.
   The data written in EEPROM can be confirmed by the [EEPROM Read] button.

[Download Sequence of the AK7755 from External EEPROM]

1. [I2CSEL] box: Set to “I2C I/F”.
2. When using MAT function,
   [CAD / MATSEL pin Select] (EEPROM tab function): Set to “MATSEL”.
3. [PDN=L/H] button: Set to “PDN = H”.
4. “EEPROM” tub setting
   4-1. When using MAT function, set MAT1-0 pins by the [MAT Select] combo box. If it is not selected by the combo box, the setting will be “00” automatically (default).
   4-2. By setting [EXTEEP pin] = “H” (or [DLS bit] = “1”), register settings, DSP programs and data can be downloaded from an external EEPROM.
   Downloaded setting is reflected to GUI by the [Read DSP] button.
   4-3. Operation when re-downloading is required
   Set [EXTEEP pin] = “H” -> “L” -> “H” (or [DLS bit] = “1” -> “0” -> “1”)
   Download begins by the above operation.

(3) “REG x ” Dialog

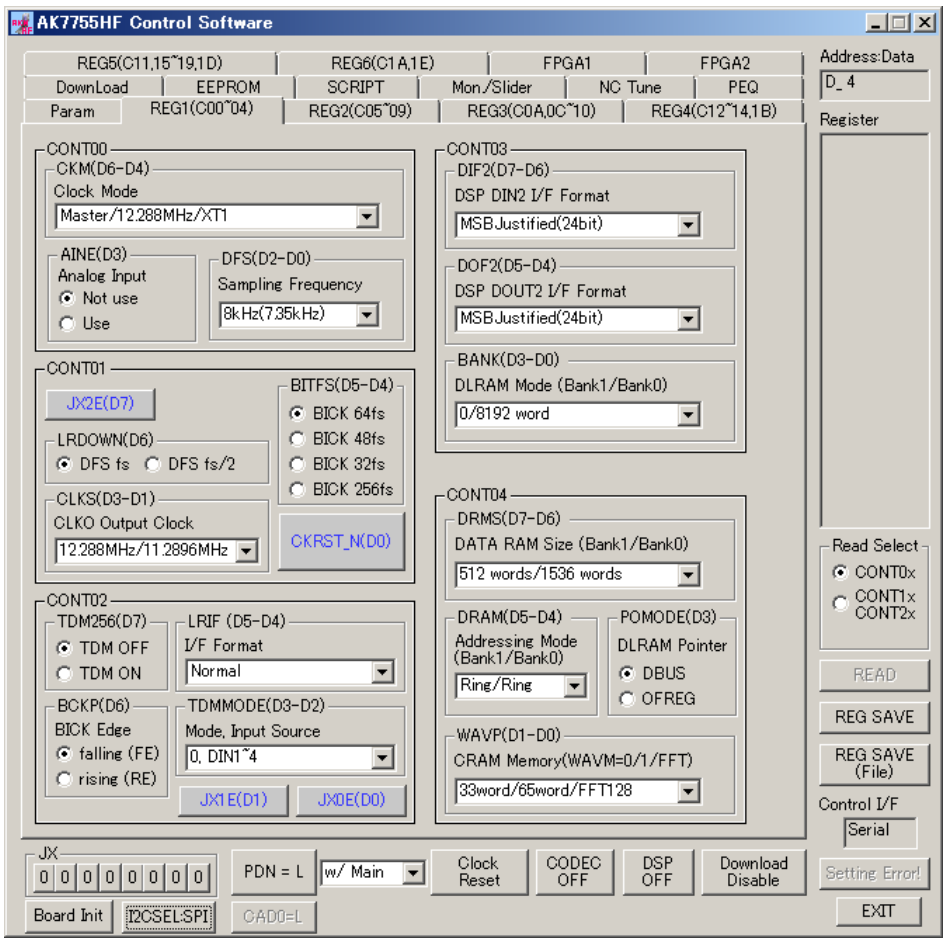


Figure 27. “REG1” Dialog

Set up the registers of the AK7755 by REG1 - REG6 dialogs.
As the checkbox is clicked, the data will be written to the AK7755 (Note 13).

Refer to a data sheet for each register.

Tab name	Setting register
REG1(C00~04)	CONT00 - CONT04
REG2(C05~09)	CONT05 - CONT09
REG3(C0A,0C~10)	CONT0A, CONT0C - CONT10
REG4(C12~14,1B)	CONT12 - CONT14, CONT1B
REG5(C11,15~19,1D)	CONT11, CONT15 - CONT19, CONT1D
REG6(C1A,1E)	CONT1A, CONT1E

Note 13. During clock reset (CKRESETN=“0”), it can write at control register (CONT00-CONT01).
The other setup can write during clock reset or DSP reset (CKRESETN bit =“0”, DSPRESETN bit =“0”).
However, control register (CONT12 - CONT19) can write in during operation.

Note 14. The value of the MICGAIN setup by DSP can be read at CONT1B on the [REG4] Dialogue. Readout becomes effective when ADRCRE bit and ADRCLE bit (CONT1A:D3, D2) are "1".

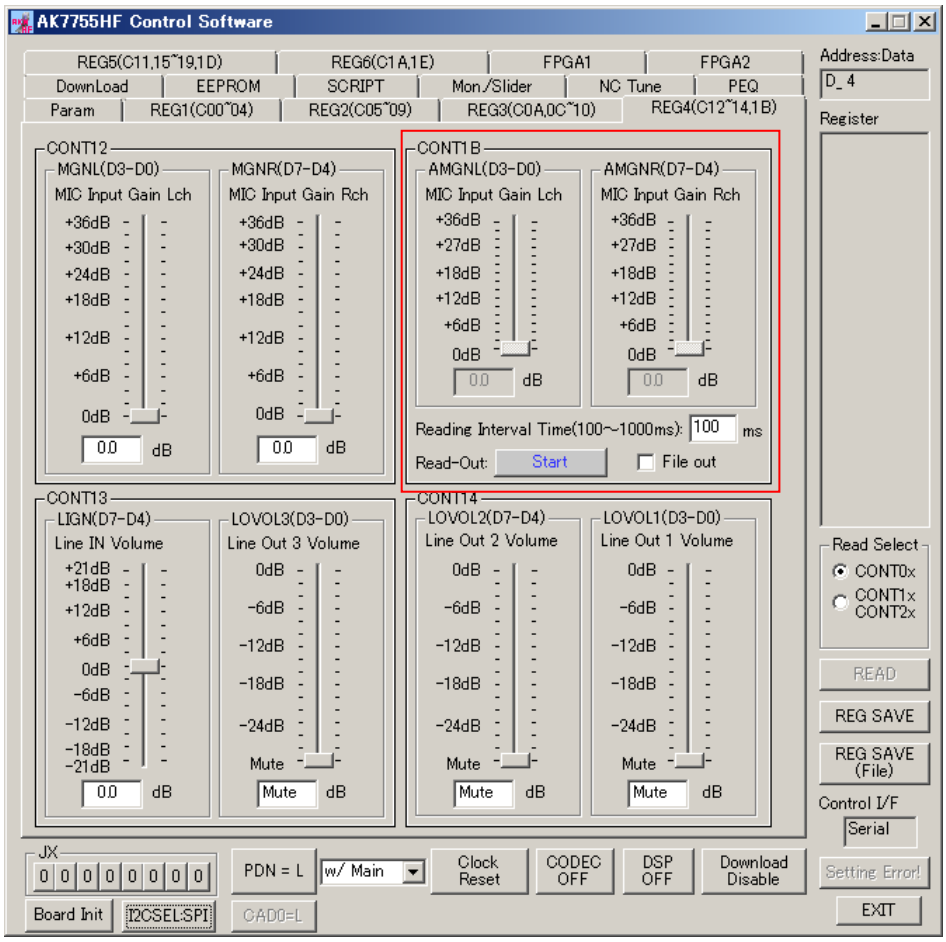


Figure 28. "REG4" Dialog

(4) “FPGA x” Dialog

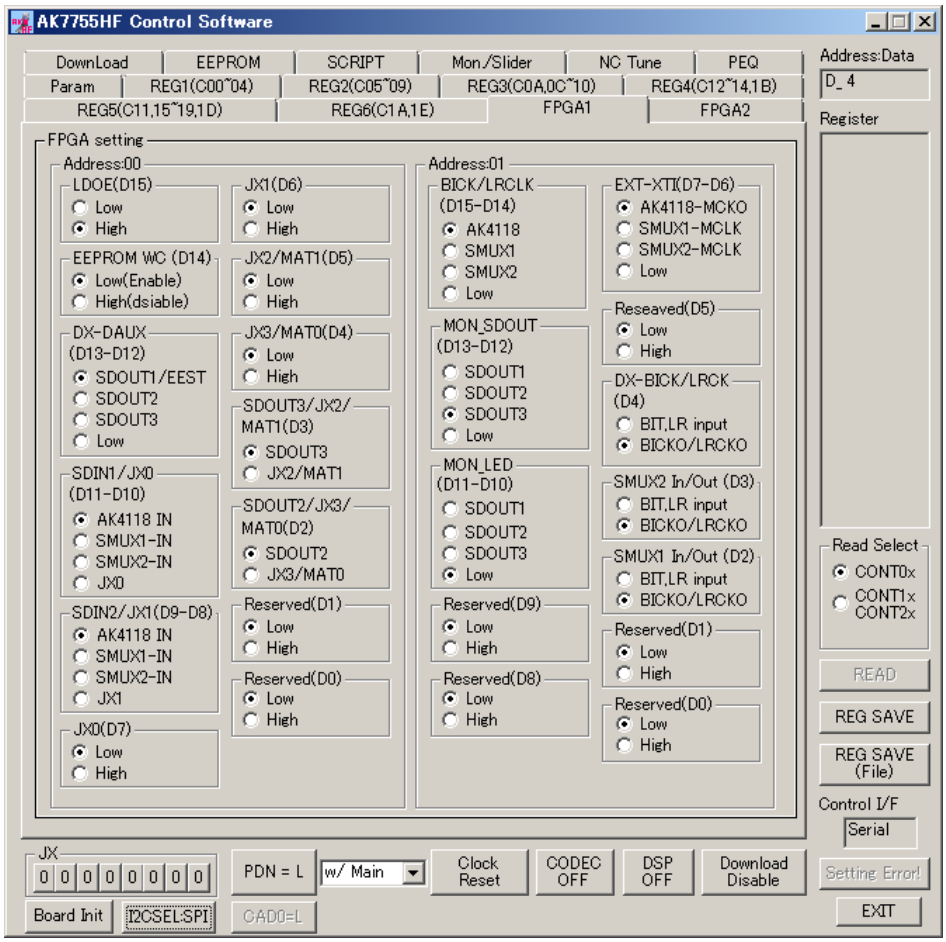


Figure 29. “FPGA1” Dialog

FPGA1/FPGA2 dialogs are used to modify the data path of the AK7755 and the setting of the AK4118A.

FPGA Setting：（**Bold type items** are default settings.）

ADDRESS ：00

Bit	Function	Description
D[15]	LDOE	Input Data source to the LDOE pin of the AK7755 0 : Low **1 : High**
D[14]	EEPROM WC	EEPROM Write Enable Selection **0 : Low(Enable)** 1 : High(Disable)
D[13:12]	DX-DAUX	Output Data Source to the DAUX of the AK4118 **00 : SDOUT1** 01 : SDOUT2 10 : SDOUT3 11 : Low
D[11:10]	SDIN1/JX0	Input Data source to the SDIN1/JX0 pin of the AK7755 **00 : AK4118 IN** 01 : SMUX1-DAT1 10 : SMUX2-DAT1 11 : JX0
D[9:8]	SDIN2/JX1	Input Data source to the SDIN2/JX1 pin of the AK7755 **00 : AK4118 IN** 01 : SMUX1-DAT1 10 : SMUX2-DAT1 11 : JX1
D[7]	JX0	Input Data source to the JX0 pin of the AK7755 **0 : Low** 1 : High
D[6]	JX1	Input Data source to the JX1 pin of the AK7755 **0 : Low** 1 : High
D[5]	JX2/MAT1	Input Data source to the JX2/MAT1pin of the AK7755 (Effective at the time of D[3]＝“1h”) **0 : Low** 1 : High
D[4]	JX3/MAT0	Input Data source to the JX3/MAT0pin of the AK7755 (Effective at the time of D[2]＝“1h”) **0: Low** 1: High
D[3]	SDOUT3/JX2/MAT1	Input / Output Setting of the SDOUT3/JX2/MAT1 pin **0 : SDOUT3 output (Xilinx←AK7755)** 1 : JX2/MAT1 input (Xilinx→AK7755)
D[2]	SDOUT2/JX3/MAT0	Input / Output Setting of the SDOUT2/JX3/MAT0 pin **0: SDOUT2 output (Xilinx←AK7755)** 1: JX3/MAT0 input (Xilinx→AK7755)
D[1:0]	Reserved	Reserved

Table 8. FPGA Setting Table 1

ADDRESS : 01

Bit	Function	Description
D[15,14]	BICK/LRCK	Input Data Source to the BICK/LRCK pin of the AK7755 **00 : AK4118-BICK/LRCK (Enabled in the D[4]=0h)** 01 : SMUX1-BICK/LRCK (Enabled in the D[2]=0h) 10 : SMUX2-BICK/LRCK (Enabled in the D[3]=0h) 11 : Low
D[13:12]	MON_SDOUT	Output setting to the monitor board 00 : SDOUT1 01 : SDOUT2 **10 : SDOUT3** 11 : Low
D[11:10]	MON_LED	Output setting to the monitor board LED 00 : SDOUT1 01 : SDOUT2 10 : SDOUT3 **11 : Low**
D[9:8]	Reserved	Reserved
D[7:6]	EXT-XTI	Input Data Source to the XTI pin of the AK7755 in Slave Mode **00 : AK4118-DX-MCKO** 01 : SMUX1-MCLK 10 : SMUX2-MCLK 11 : Low
D[5]	Reserved	Reserved
D[4]	DX-BICK (AK4118<=>AK7755)	Input / Output Setting of the AK4118's BICK/LRCK pin 0 : BICK/LRCK input (AK4118→AK7755) **1 : BICK/LRCK output (AK4118←AK7755)**
D[3]	SMUX2 In/Out (SMUX2<=>AK7755)	Input / Output Setting of the SMUX PORT2's BICK/LRCK pin 0 : BICK/LRCK input (SMUX2→AK7755) **1 : BICK/LRCK output(SMUX2←AK7755)**
D[2]	SMUX1 In/Out (SMUX1<=>AK7755)	Input / Output Setting of the SMUX1 PORT1's BICK/LRCK pin 0 : BICK/LRCK input (SMUX1→AK7755) **1 : BICK/LRCK output(SMUX1←AK7755)**
D[1:0]	Reserved	Reserved

Table 9. FPGA Setting Table 2

ADDRESS : 02

Bit	Function	Description
D[15:14]	SMUX2-DOUT	Output Data Source to the DOUT pin of the SMUX PORT2 **00 : SDOUT1** 01 : SDOUT2 10 : SDOUT3 11 : Low
D[13:12]	SMUX1-DOUT	Output Data Source to the DOUT pin of the SMUX PORT1 **00 : SDOUT1** 01 : SDOUT2 10 : SDOUT3 11 : Low
D[11,10]	DX-CLKO	Input Clock Source to the XTI pin of the AK4118 **00 : AK7755 CLKO** 01 : SMUX1-MCLK 10 : SMUX2-MCLK 11 : Low
D[9:7]	Reserved	Reserved
D[6:5]	SMUX2-MCLK	Input / Output setting and Output Data Source of the SMUX 00 : MCLK input **01 : AK7755-CLKO** 10 : AK4118-DX-MCKO 11 : SMUX1-MCLK
D[4:3]	SMUX1-MCLK	Input / Output setting and Output Data Source of the SMUX 00 : MCLK input **01 : AK7755-CLKO** 10 : AK4118- DX-MCKO 11 : SMUX2-MCLK
D[2:0]	Reserved	Reserved

Table 9. FPGA Setting Table 3

AK4118A Setting： （**Bold type items** are the default setting.）

Function	Description
MCLK	MCLK Setting of the AK4118A **00: 256fs** 01: 256fs 10: 512fs 11: 128fs
CM	CM Mode Setting of the AK4118A 00: CM = 00 01: CM = 01 **10: CM = 10** 11: CM = 11
DIF	AK4118 DIF Mode 000: 16bit Right(O) 001: 18bit Right(O) 010: 20bit Right(O) 011: 24bit Right(O) **100: 24bit Left(O)** 101: 24bit I^2S(O) 110: 24bit Left(I) 111: 24bit I^2S(I)

Table 10. AK4118A Setting Table

PDN pin = H: AK4118A power up
L: AK4118A power down

(5) “SCRIPT” Dialog

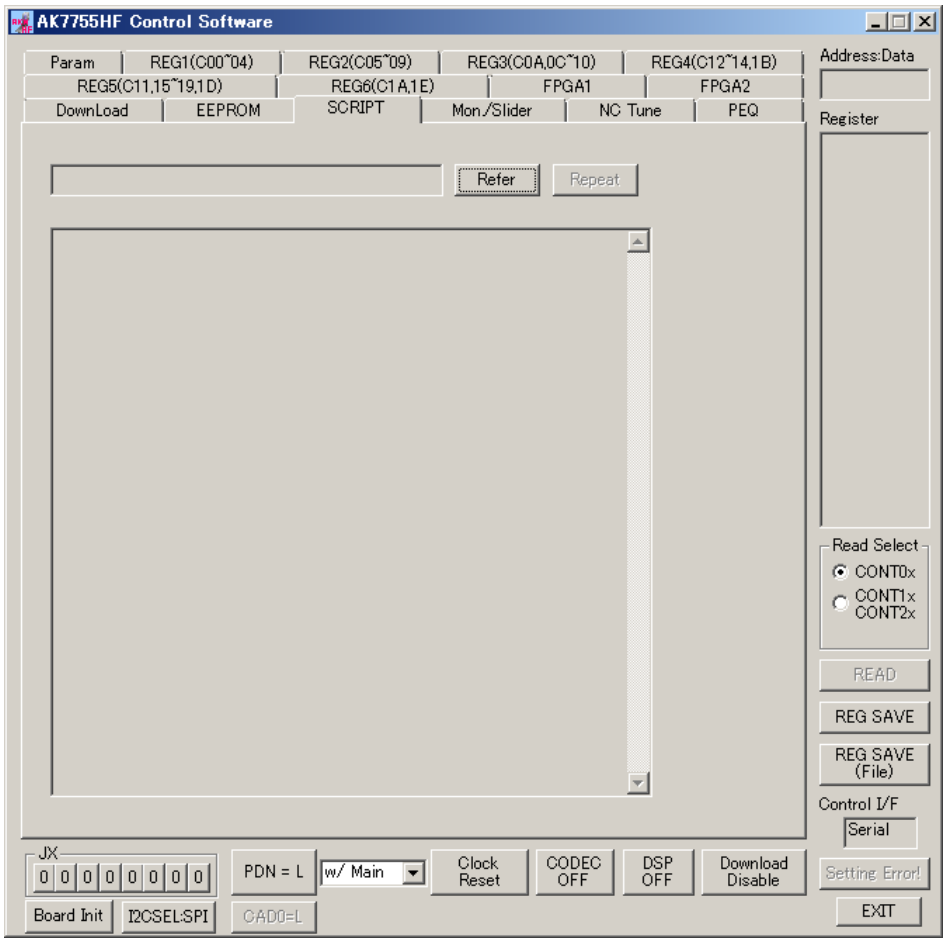


Figure 30. “SCRIPT” Dialog

[Refer]: When a script file is selected, it will be executed.
[Repeat]: The selected script file will be executed once again.

Command	Description
[SCRIPT]	Header of script file. A data error will be detected without this header.
; Comment	The line following to ";" is recognized as comment and ignored.
W,<address>,<data> W,0xC0,0x00	Register Write. Both address and data are byte (8bit) assigned.
WL,<command>,<address>,<data>,… WL,0x82,0x0022,0x4000,0x4000,0x4000	Continuous Data Write. This command can be used during CRAM run. The command is byte (8bit) assigned and the following data is word (16bit) assigned.
WS,<command>,<address>,<data>,… WS,0x81,0x00,0x22,0x40,0x00,0x40,0x00	Continuous Data Write. This command can be used during CRAM run. The command, address and data are byte (8bit) assigned.
RI: H / RI: L RP : H / RP : L RM : H / RM : L RC: H / RC: L RS: H / RS: L RD: H / RD: L	Initial Reset. (PDN pin) Power SW Reset. Register Reset. Clock Reset. CODEC Reset. DSP Reset.
D,<address>,<data>	AK4118A Write Command
X,<address>,<data>	FPGA Register Write Command
P,<message>	Displays a message and pose the script.
T,<wait> T,50mS	Wait some micro sec. 50msec wait.
LP:<filename>	Program file download to the DSP.
LC:<filename>	Coefficient file download to the DSP.
LO:<filename>	Off-set file download to the DSP.

Table 12. Script Command Table

(6) “Mon/Slider” Dialog

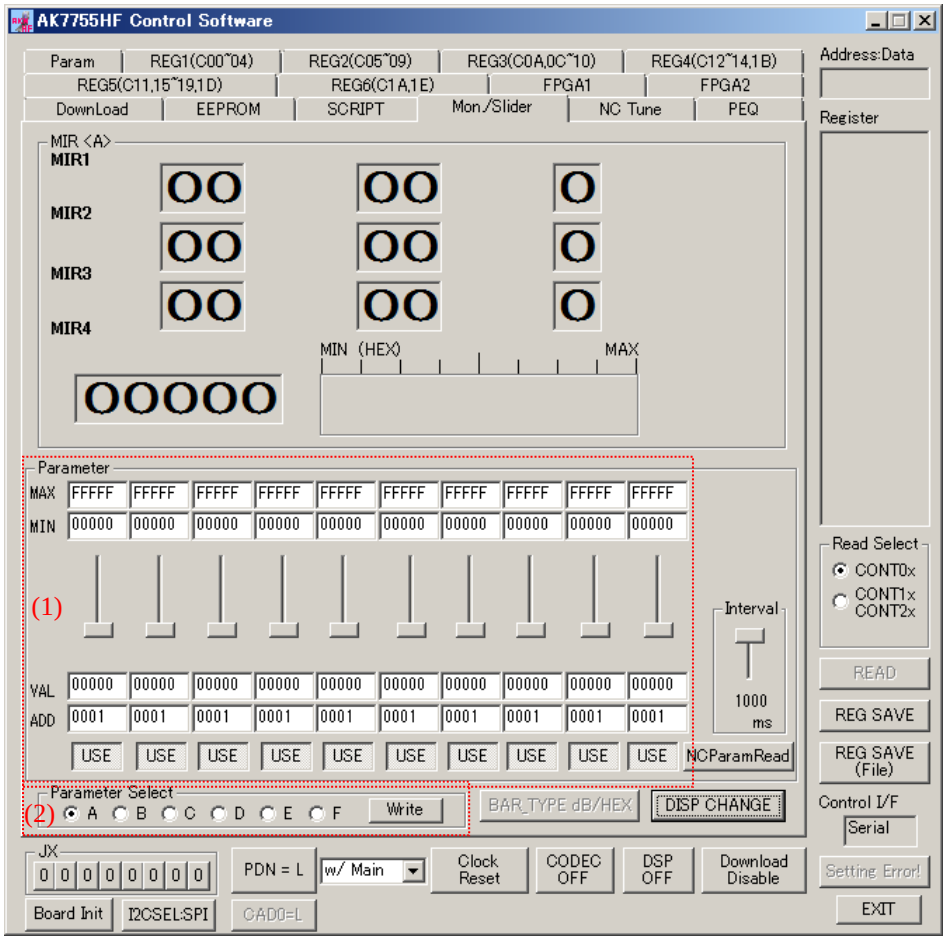


Figure 31. “Mon/Slider” Dialog

With this GUI, it is possible to make adjustment of ten CRAM parameters in RUN state. (A - F: 10 * 6)

(1) Push down the “USE” button to write each operation setting to the DSP.
Write the address to “ADDR”. → Enter.
Set the range of the slide bar to “MAX” and “MIN”. (Usually 7FFFFF - 000000)
Set the value to “VAL”. → Enter (Slide bar is also available for this setting.)

(2) From A to F, six sets of parameter settings are available.

[CRAM Parameter Adjustment]

Set the parameters in CRAM to adjust Hands Free setting. In this instruction manual, CRAM addresses are expressed as C (xxxx). Address = 04Ch is shown below as an example.

Example:

C(04Ch)	CRAM Address 04Ch

A corresponding example to the CRAM file is shown below.

```
059F00 ;04B MIC1_DELAY Read pointer
008000 ;04C FES_IN_ATT 0dB
004000 ;04D MIC_IN_ATT -6dB
008000 ;04E FES_OUT_ATT +0dB
```

Figure 32. AK7755 CRAM File Format

The figure above shows that 008000h is stored to C(04Ch) when this file is downloaded.

(7) “NC Tune” Dialog

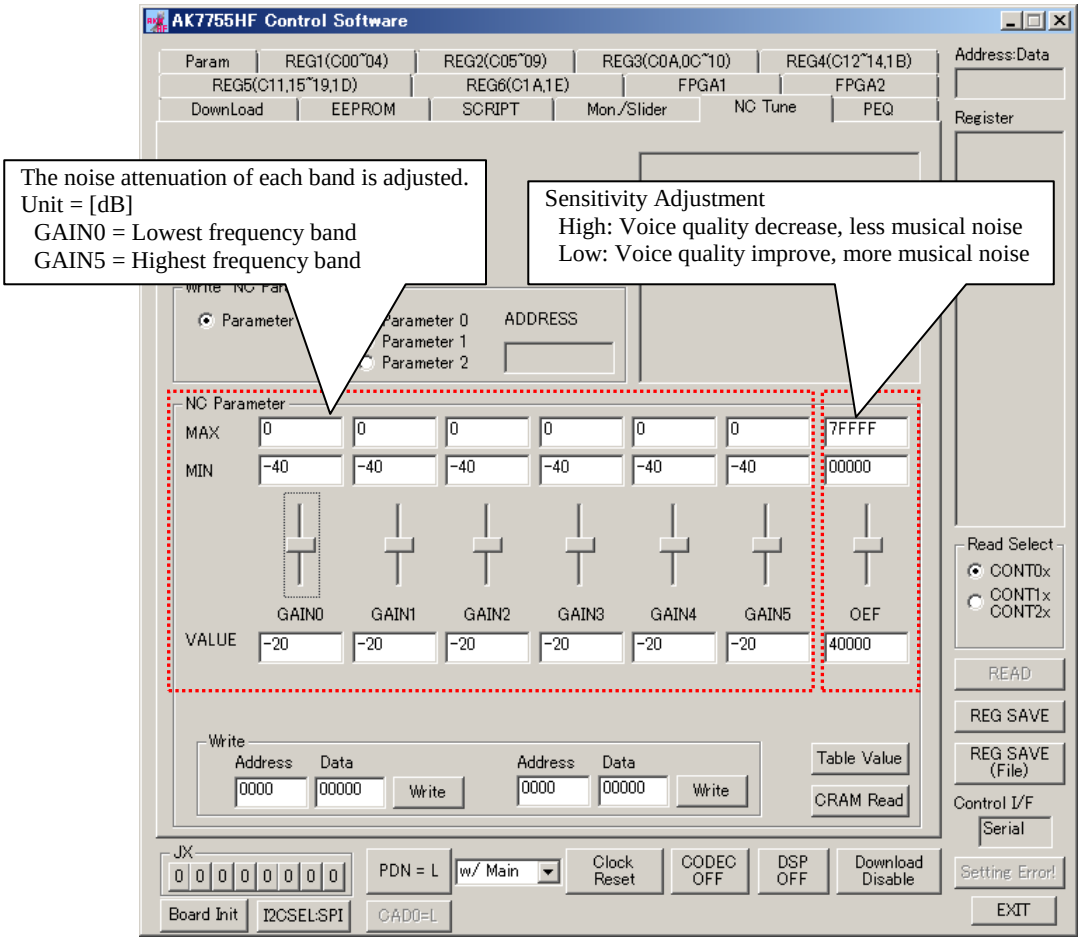


Figure 33. “NC Tune” Dialog

The noise canceller sets optional noise attenuation for six divided voice bands. This noise cancel adjustment is made with the real time NC parameter adjustment function of GUI software as shown in the following diagram.

Note 15. There is a case that an error masse “OVER!!(SN)” is displayed under value boxes. It is recommended to avoid this error message because the NC performance is at the limit so that there might be a difference between the setting value and the actual noise cancel operation.

(8) “PEQ” Dialog

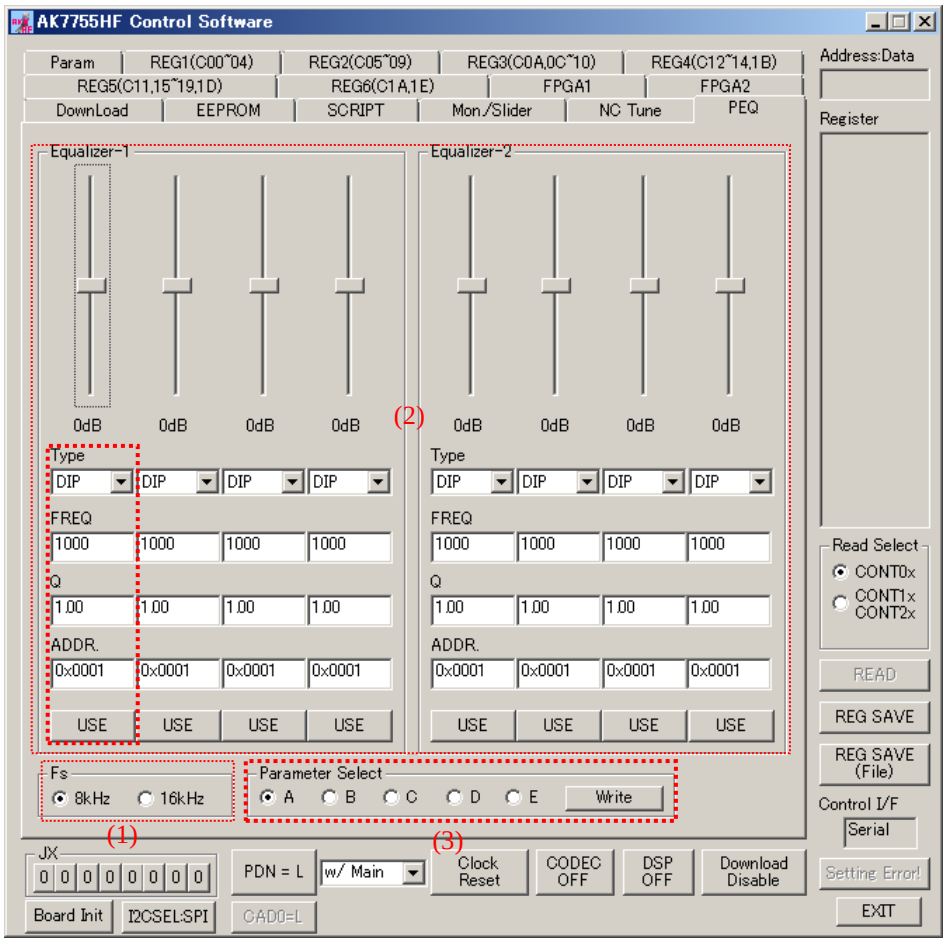


Figure 34. “PEQ” Dialog

40 bands (8 bands * 5) adjustments can be made and RUN time adjustment is available by GUI.

Six types of filters can be selected on GUI software.
DIP(Boost and decompress for specific frequency), LPF12(Low Pass Filter 12dB/oct), HPF12(High Pass Filter 12dB/oct), LPF6(Low Pass Filter 6dB/oct), HPF6(High Pass Filter 6dB/oct), Att(Gain Adjustment)

[Parametric Equalizer Settings]
(1) Select fs setting. (Do not change it during Run state.)
(2) Push down the “USE” button to write operation settings to the DSP.

Set the initial address of the PEQ band that need to be modified, to “ADDR”. → Enter
Use the “Type” pull-down menu box to select a filter type.
Set the cutoff frequency of the filter to “FREQ”. → Enter
Set the quality factor of the filter to “Q”. → Enter
When filter type is “DIP” or “ATT”, the slid bar is available for gain setting.
(Filter OFF Setting: Type = DIP, Gain = 0dB)
(3) From A to E, there are five sets of eight bands setting are available.

Note 16. The “PEQ” tab screen indicates only setting results of this window. When re-downloading a CRAM setting, the AK7755 operates on the down loaded CRAM setting that could differ from the setting shown in this screen.

7. Revision History

Date (yy/mm/dd)	Manual Revision	Board Revision	Reason	Page	Contents
13/11/25	KM115400	0	First edition	-	
13/12/06	KM115401	0	Change	38	Circuit diagram was changed. Pin assignments of U1 device (29 pin and 30 pin).
14/06/03	KM115402	1	Change	17-35	Control Soft Manual was changed.
				38-54	Circuit diagram and pattern layout were changed. Board Rev.0 -> 1
14/10/14	KM115403	2	Change	38, 41	Circuit diagram was changed. C4, C5, C6, C7, C8: Short -> 2.2uF C41, C44, C45, C48, C49: 2.2uF -> Short
				38-54	Circuit diagram and pattern layout were changed. Board Rev.1 -> 2
15/06/11	KM115404	2	Change	17-35	Control Soft Manual was changed.

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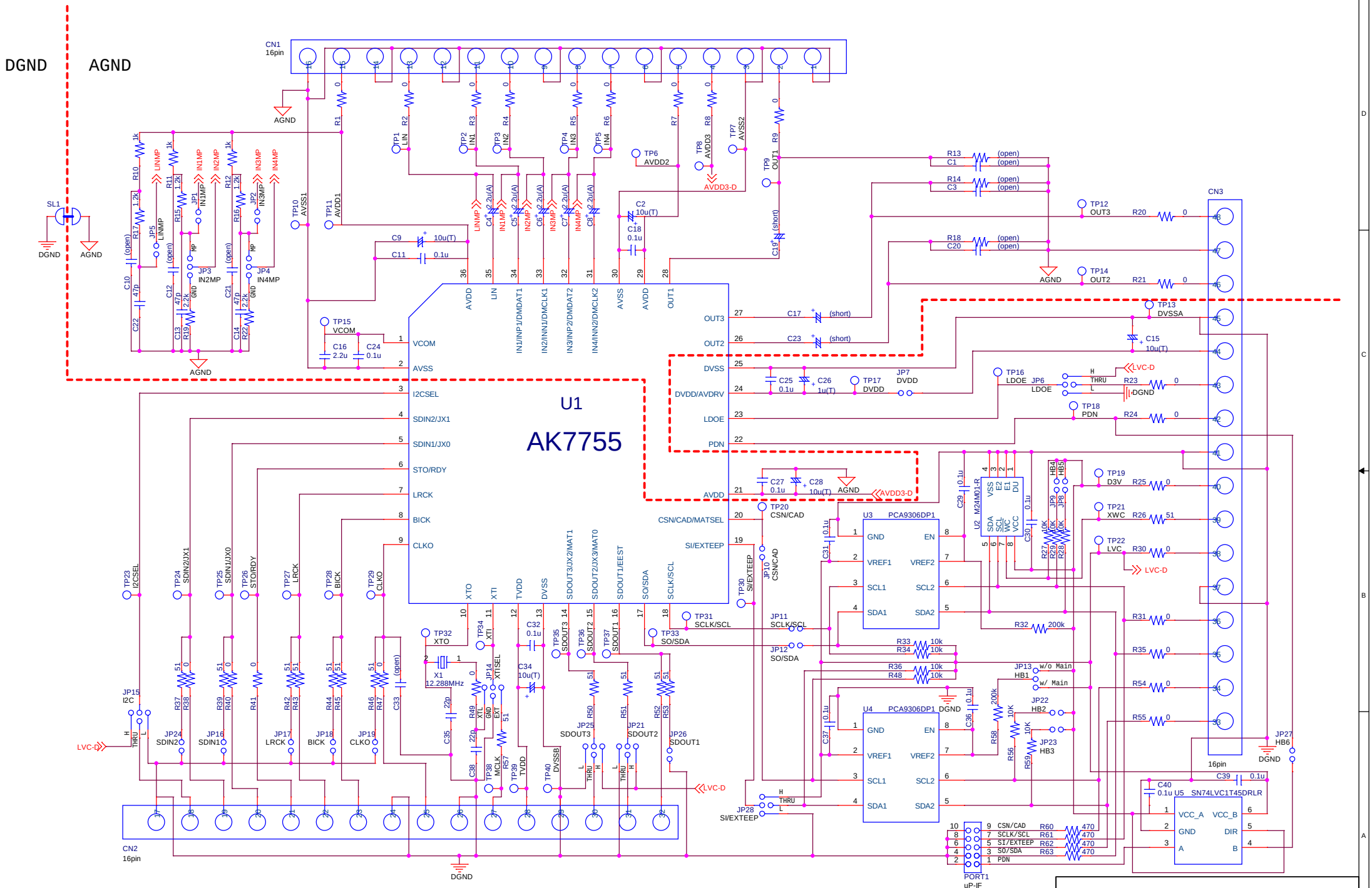

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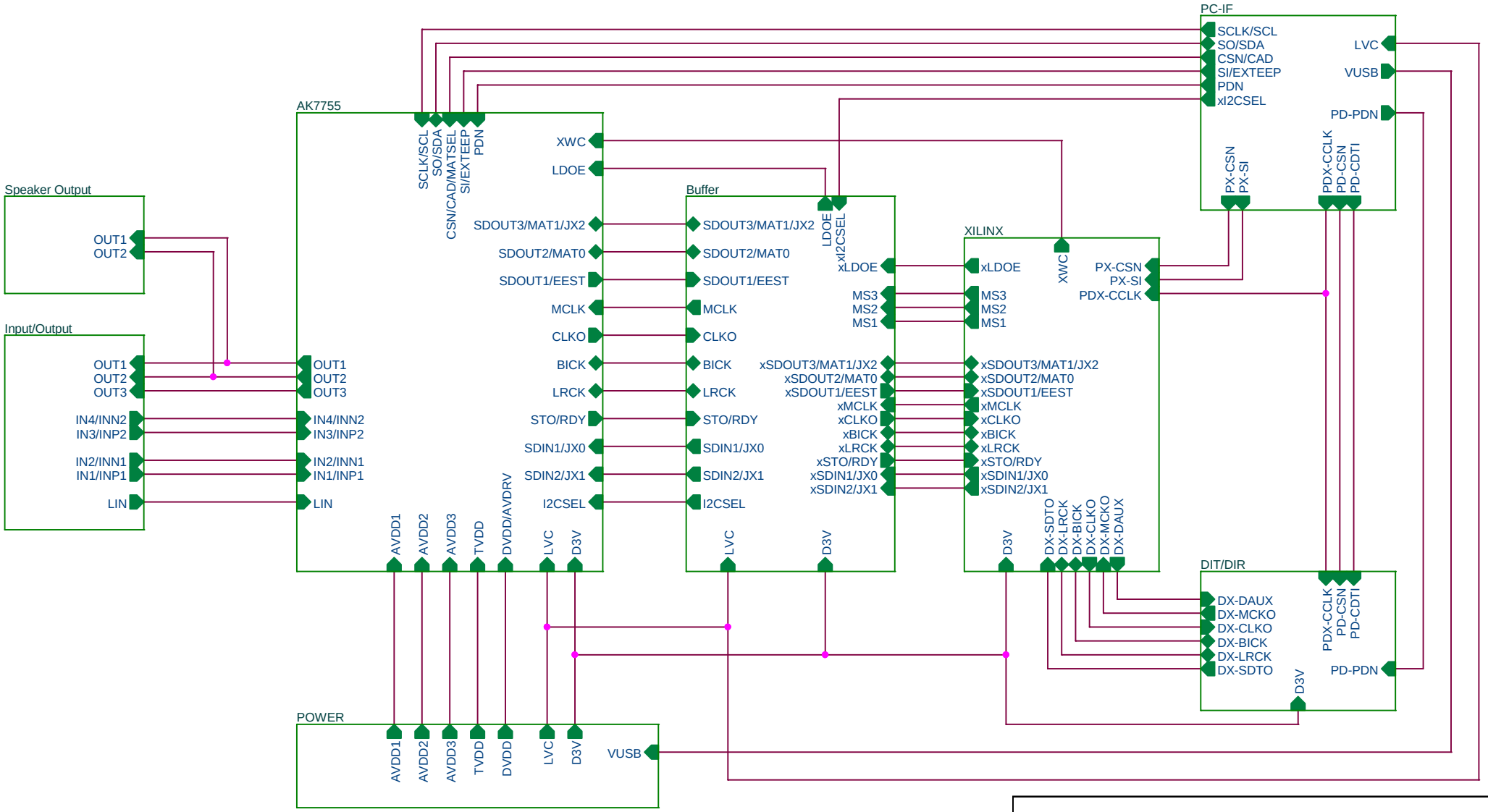
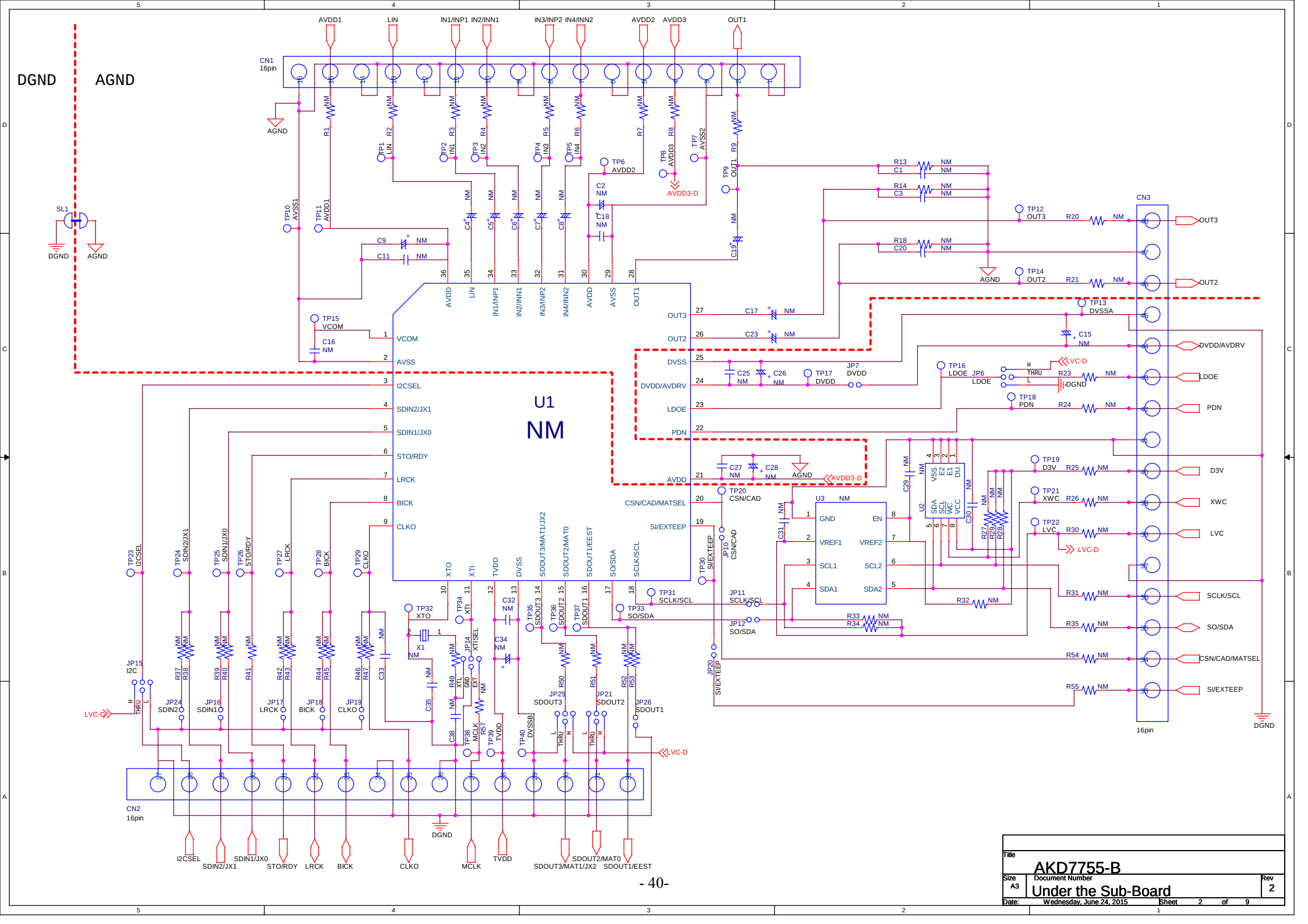
Size A3	Document Number AKD7755-BHB	Rev 2
Date: Wednesday, June 24, 2015	Sheet 1 of 1	



Title	AKD7755-B	
Size A4	Document Number Top Sheet	Rev 2
Date: Wednesday, September 24, 2014	Sheet 1 of 9	



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Size A3	Document Number Under the Sub-Board	Rev 2
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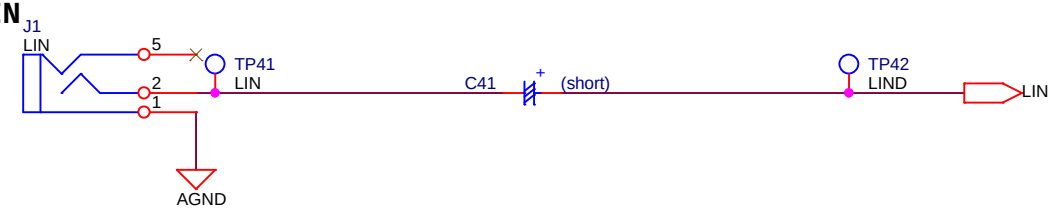

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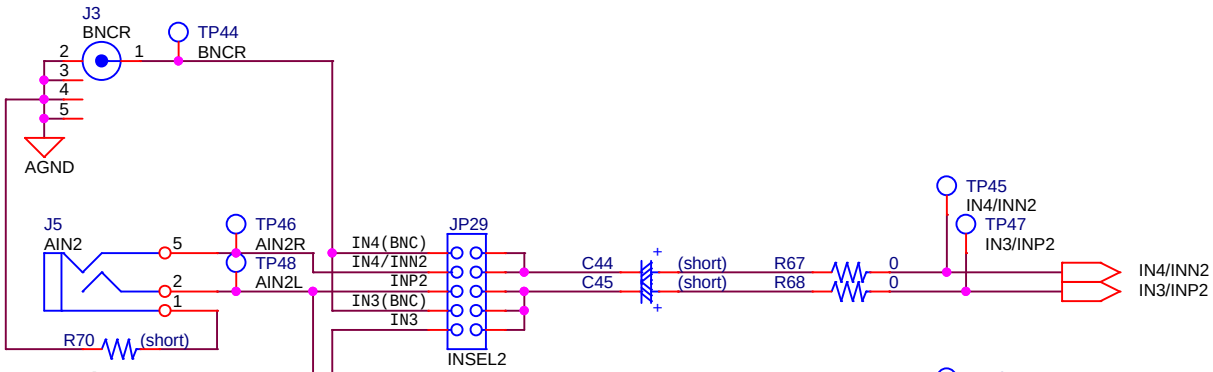

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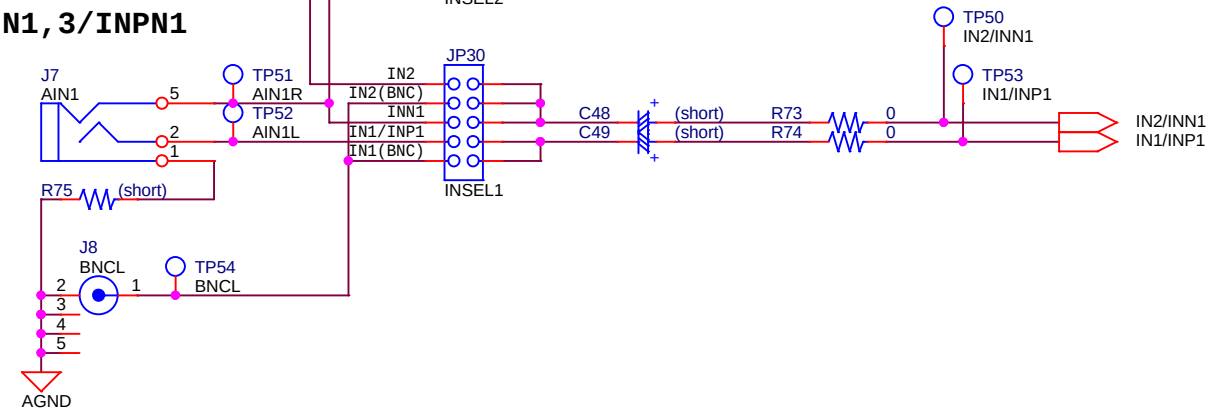

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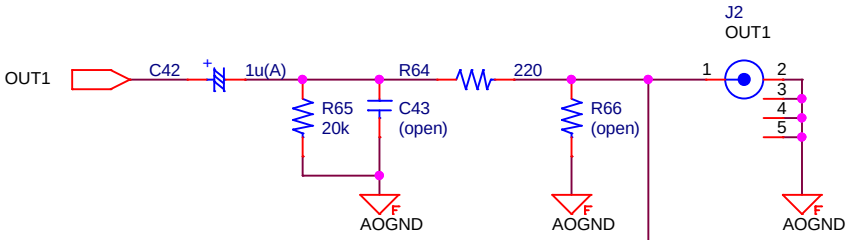

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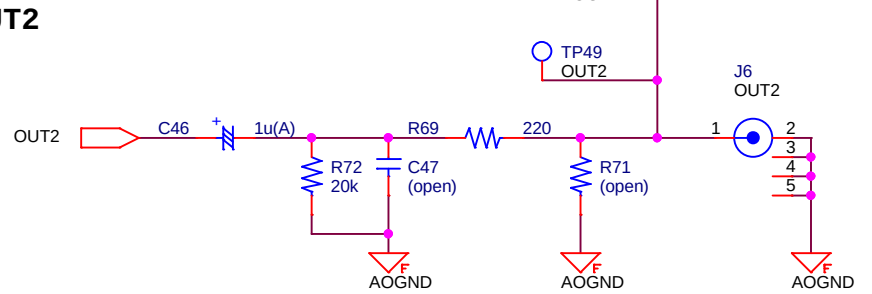

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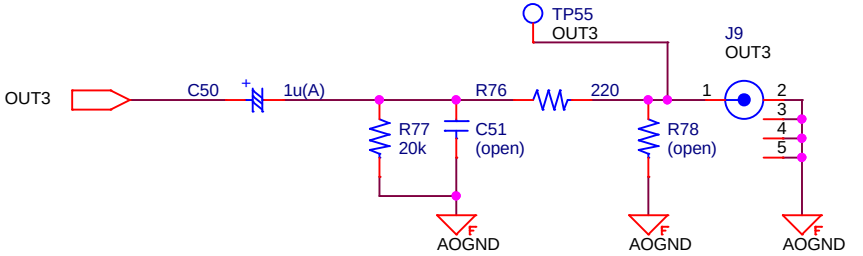

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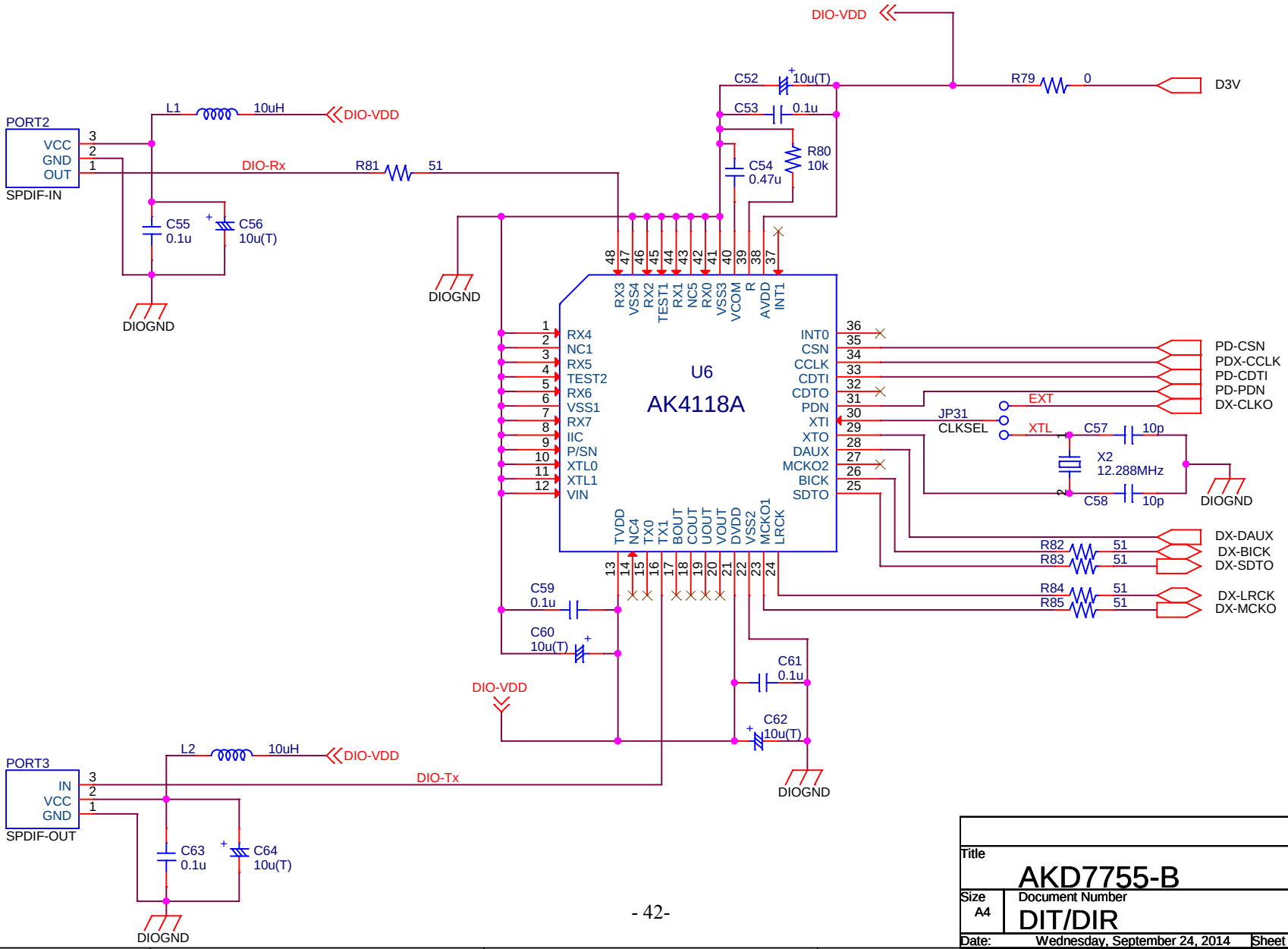
Size A4	Document Number Input/Output	Rev 2
Date: Wednesday, September 24, 2014	Sheet 3 of 9	



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Size A4	Document Number DIT/DIR	Rev 2
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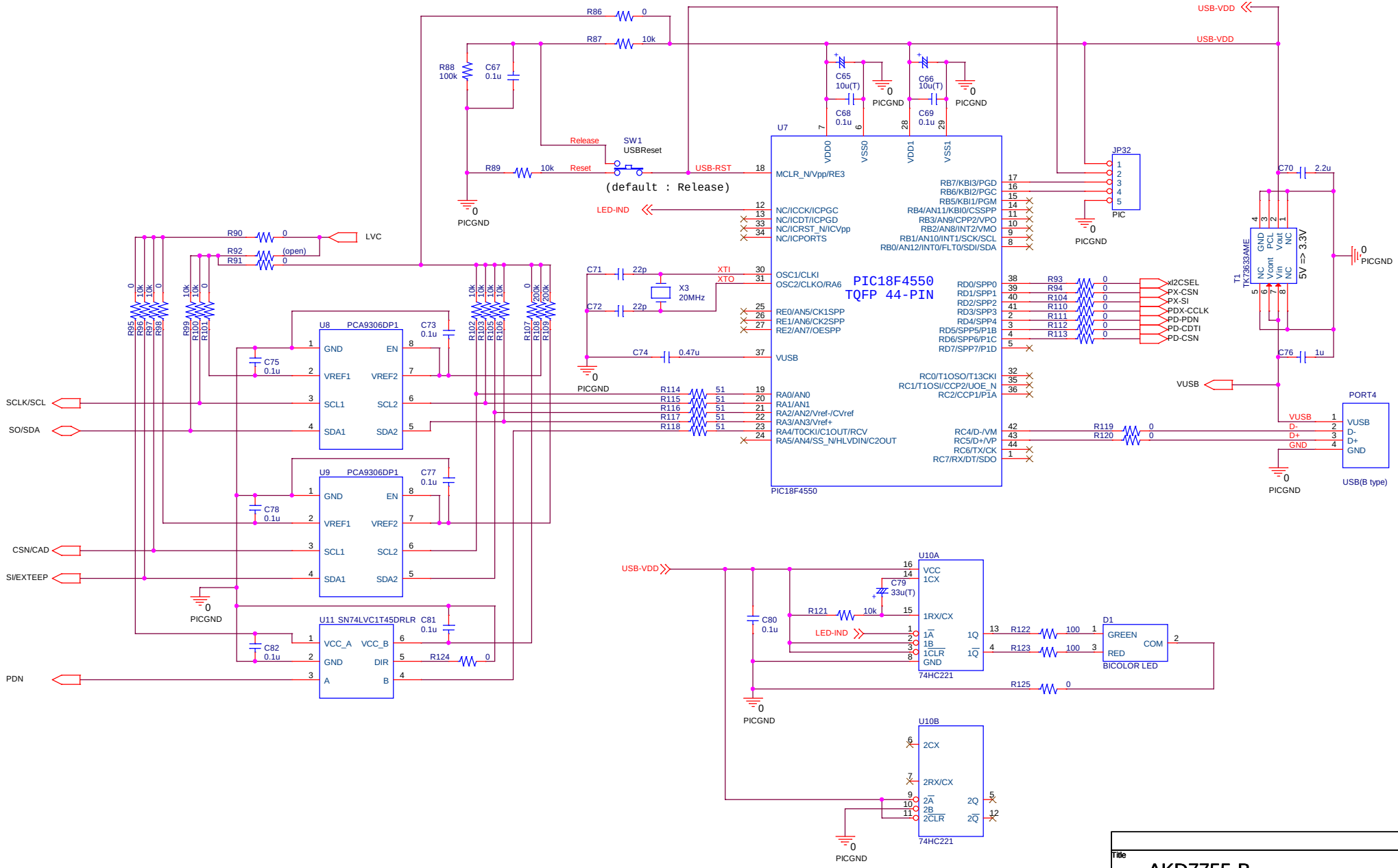

Title	AKD7755-B	
Size A3	Document Number PIC-IF	Rev 2
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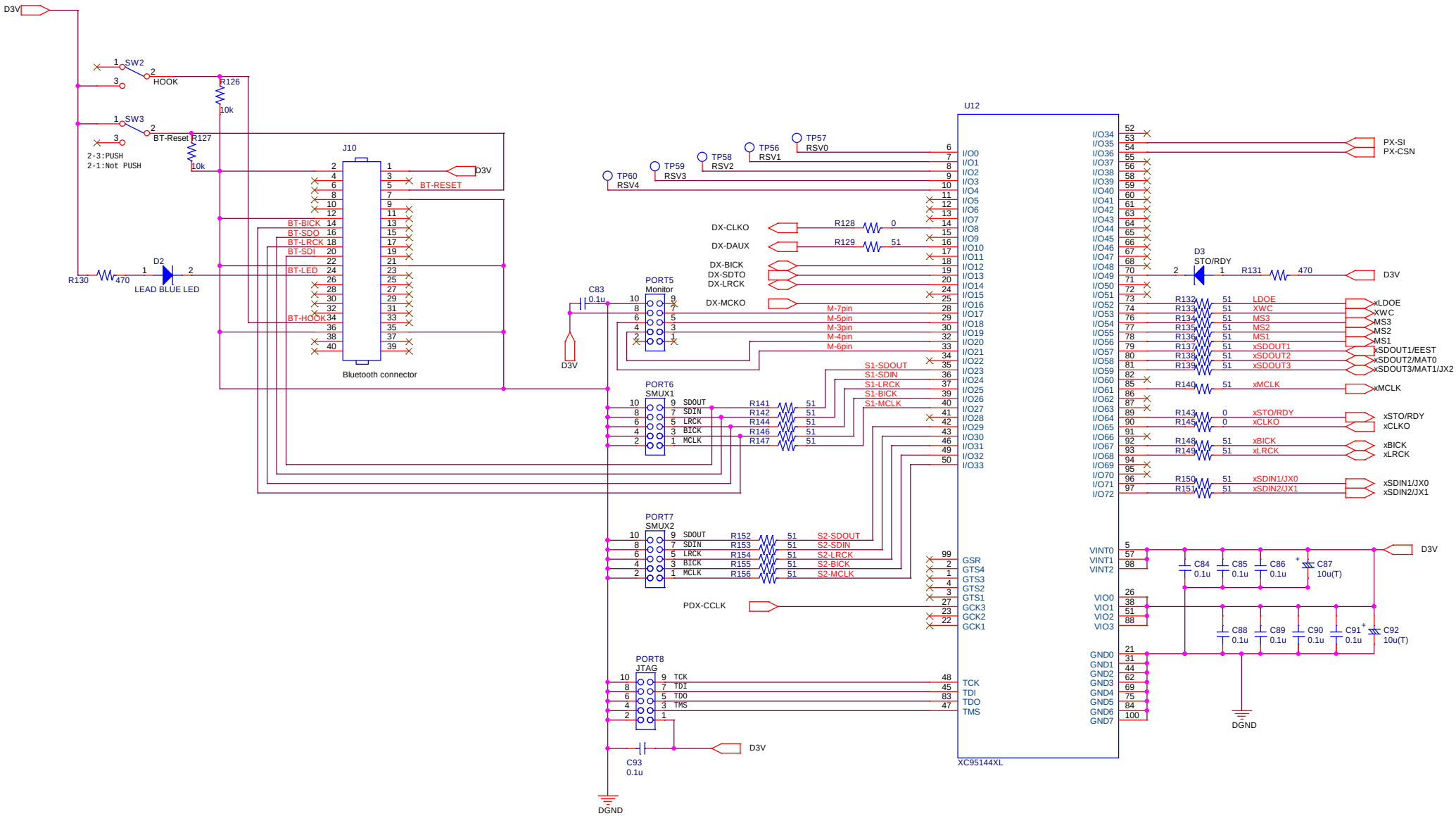

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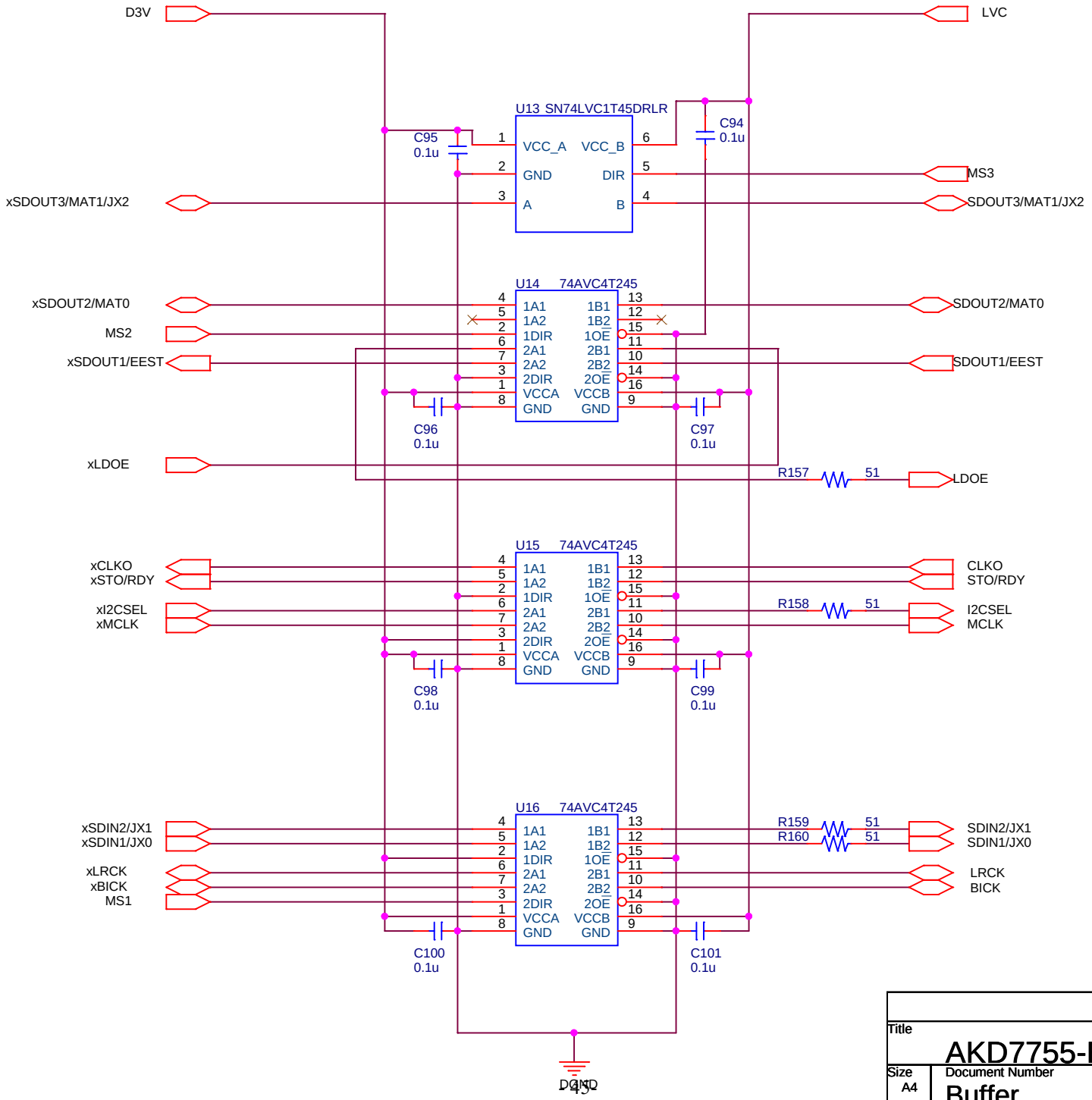

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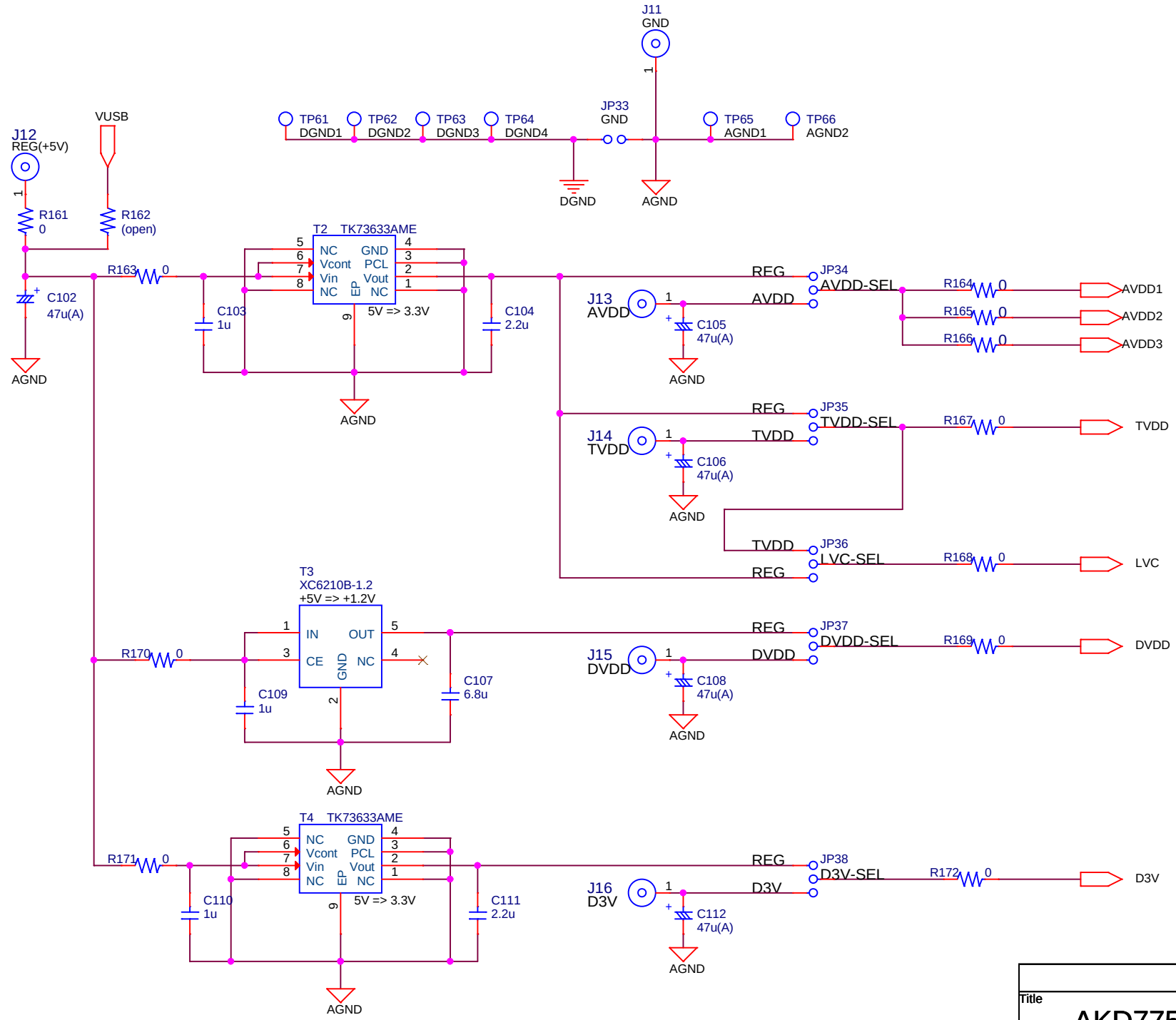

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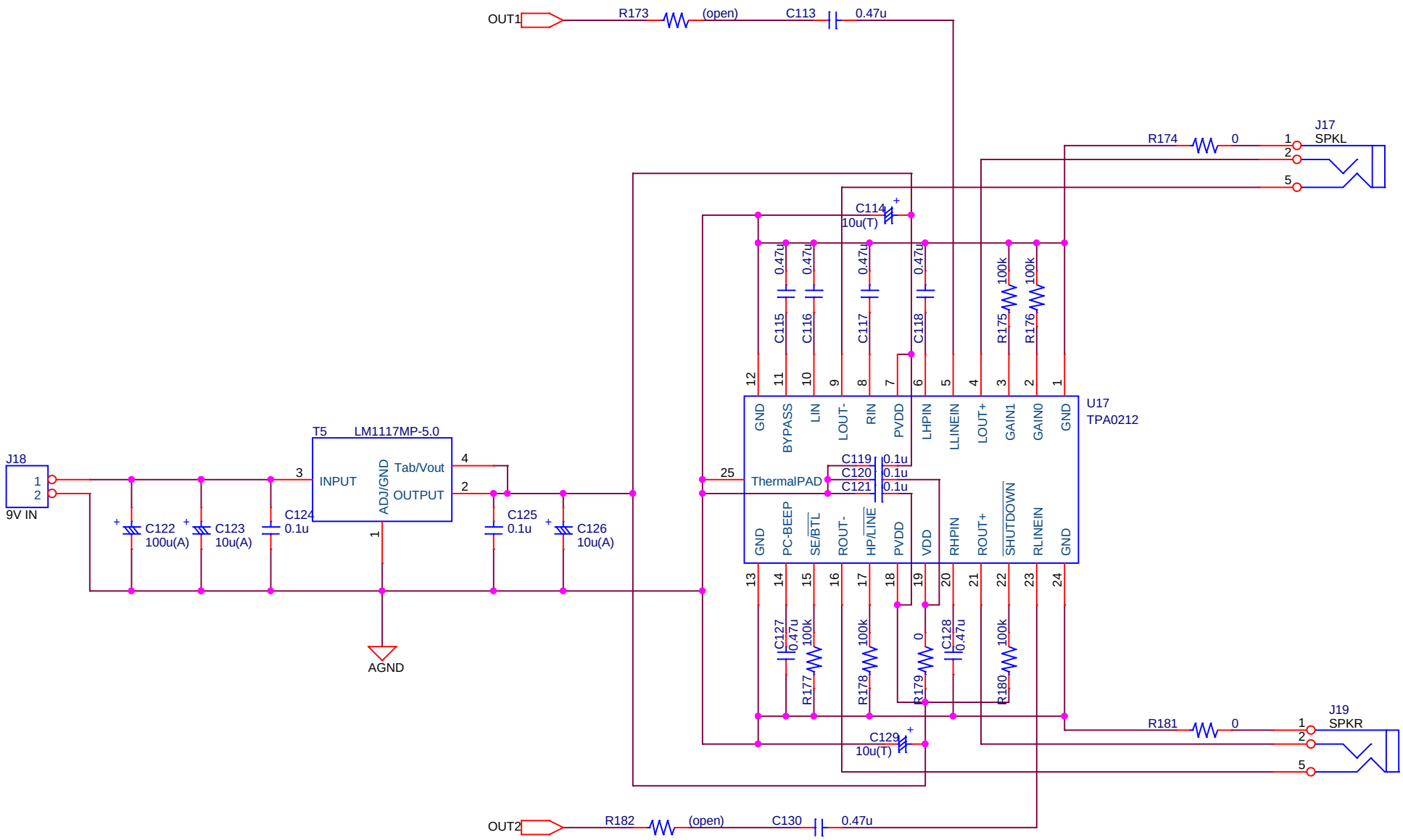
Date: Wednesday, September 24, 2014	Sheet 8 of 9	



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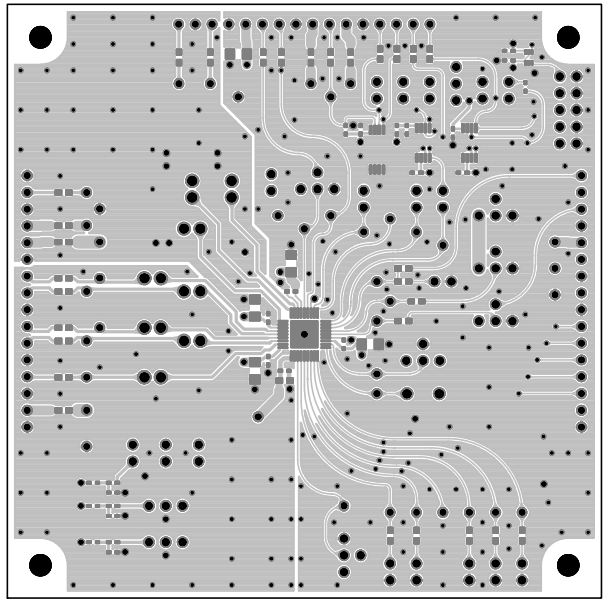
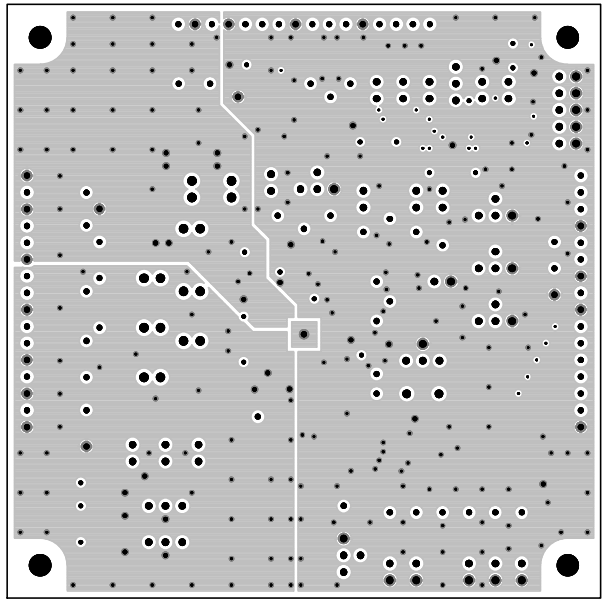
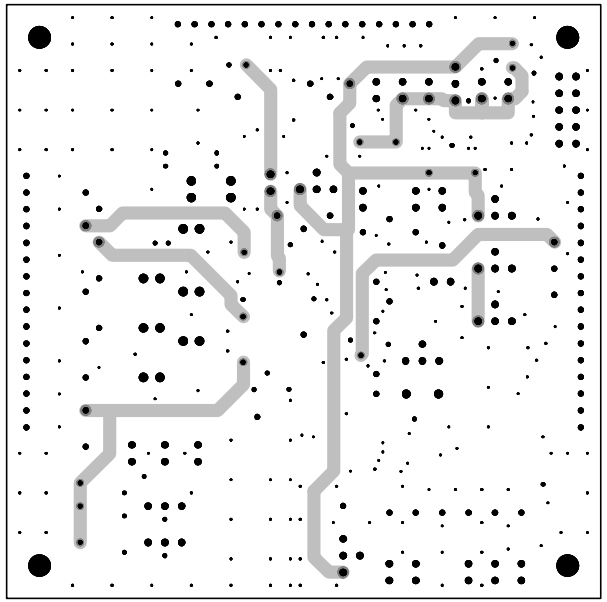
Size A4	Document Number Speaker Output	Rev 2
Date: Wednesday, September 24, 2014	Sheet 9 of 9	



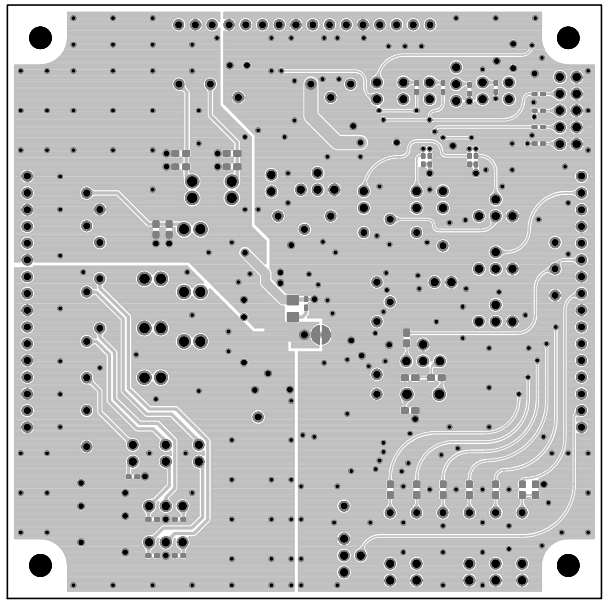
AKD7755-BHB **Rev.2**
Lay1



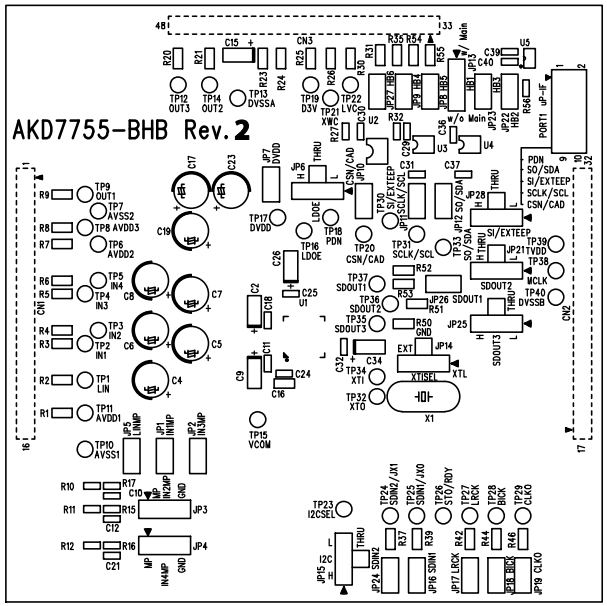
AKD7755-BHB **Rev.2**
Lay2



AKD7755-BHB **Rev.2**
Lay3



AKD7755-BHB **Rev.2**
Lay4



AKD7755-BHB **Rev.2**
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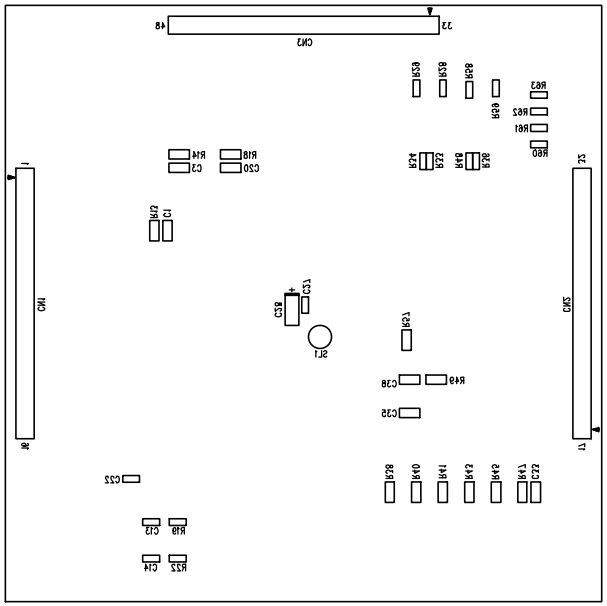

AKD7755-BHB **Rev.2**
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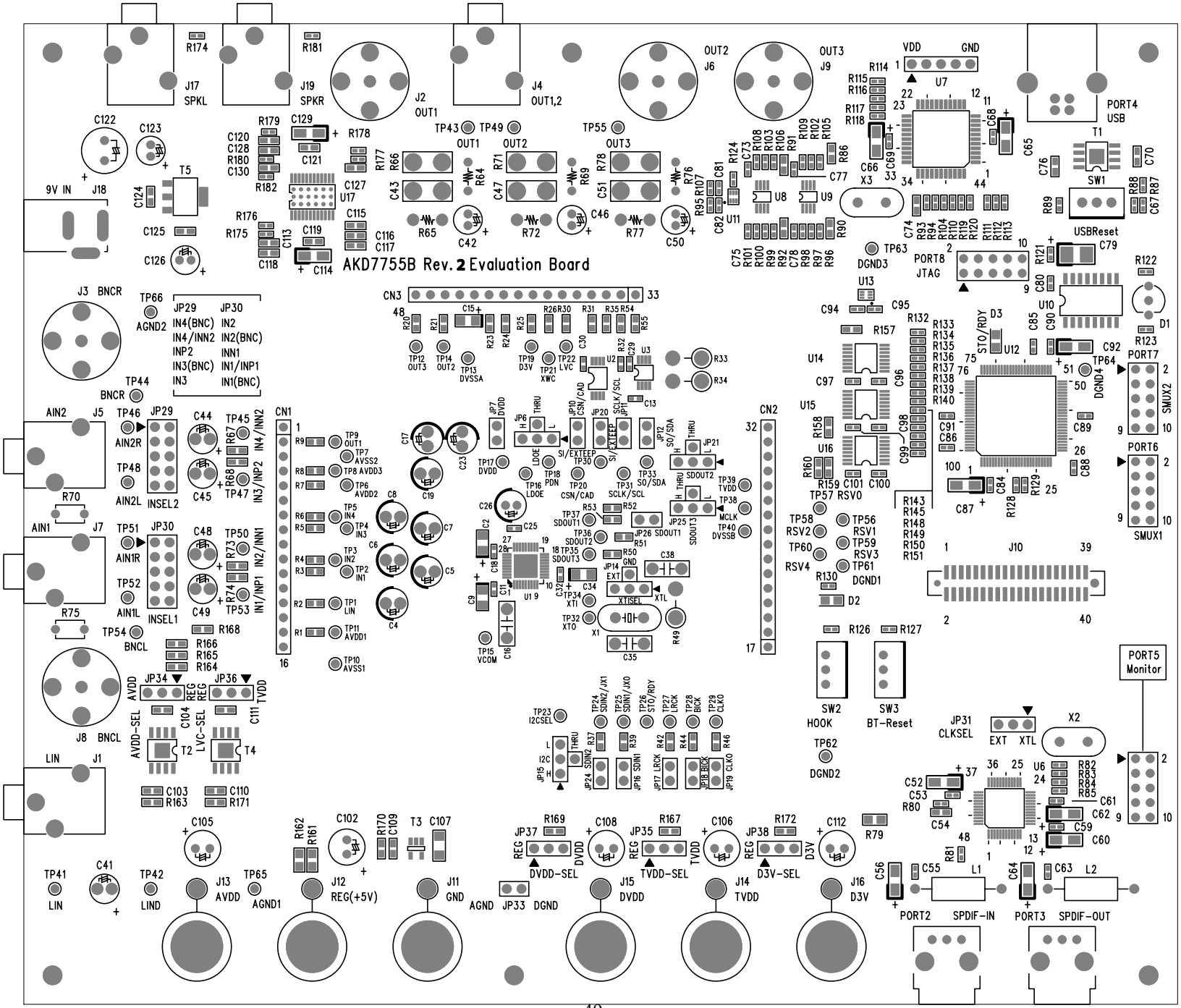
AKD7755B Rev.2 Evaluation Board
J17 SPKL
J19 SPKR
J2 OUT1
J4 OUT1,2
J6 OUT2
J9 OUT3
PORT4 USB
PORT8 JTAG
USBReset
SW1
9V IN J18
J3 BNCR
J5 AIN2
J7 AIN1
J8 BNCL
J1 LIN
AIN2R
AIN2L
AIN1R
AIN1L
BNCR
BNCL
LIN
INSEL2
INSEL1
JP29
JP30
IN4(BNC) IN2
IN4/INN2 IN2(BNC)
INP2 INN1
IN3(BNC) IN1/INP1
IN3 IN1(BNC)
AGND2
CN1
CN2
CN3
JP34 AVDD REG
JP36 TVDD REG
AVDD-SEL
LVC-SEL
JP37 DVDD REG
JP35 TVDD REG
JP38 D3V REG
DVDD-SEL
TVDD-SEL
D3V-SEL
J13 AVDD
J12 REG(+5V)
J11 GND
J15 DVDD
J14 TVDD
J16 D3V
AGND JP33 DGND
TP41 LIN
TP42 LIND
TP65 AGND1
SW2 HOOK
SW3 BT-Reset
TP62 DGND2
JP31 CLKSEL
EXT XTL
X2
PORT5 Monitor
PORT2 SPDIF-IN
PORT3 SPDIF-OUT
SMUX1
SMUX2
PORT6
PORT7
TP63 DGND3
TP64 DGND4
TP57 RSV0
TP58 RSV2
TP56 RSV1
TP60
TP59 RSV3
RSV4
TP61 DGND1
JP14 EXT XTL XTSEL
JP15 I2C
JP2 SO/SDA
JP10 CSN/CAD
JP11 SCLK/SCL
JP20 SI/EXTEEP
JP6 LDOE
JP7 DVDD
JP21 SDOUT2
JP25 SDOUT3
JP26 SDOUT1
JP24 SDIN2/JX1
JP16 SDIN1/JX0
JP17 LRCK
JP18 BICK
JP19 CLKO
TP23 I2CSEL
TP24 SDIN2/JX1
TP25 SDIN1/JX0
TP26 STO/RDY
TP27 LRCK
TP28 BICK
TP29 CLKO
TP30 SI/EXTEEP
TP31 SCLK/SCL
TP33 SO/SDA
TP35 SDOUT3
TP36 SDOUT2
TP37 SDOUT1
TP38 MCLK
TP39 TVDD
TP40 DVSSB
TP34 XTI
TP32 XTO
TP15 VCOM
TP16 LDOE
TP17 DVDD
TP18 PDN
TP20 CSN/CAD
TP22 LVC
TP19 D3V
TP21 XWC
TP12 OUT3
TP14 OUT2
TP13 DVSSA
TP9 OUT1
TP7 AVSS2
TP8 AVDD3
TP6 AVDD2
TP5 IN4
TP4 IN3
TP3 IN2
TP2 IN1
TP1 LIN
TP11 AVDD1
TP10 AVSS1
TP43 OUT1
TP49 OUT2
TP55 OUT3
TP44 BNCR
TP46 AIN2R
TP48 AIN2L
TP51 AIN1R
TP52 AIN1L
TP54 BNCL
TP45 IN4/INN2
TP47 IN3/INP2
TP50 IN2/INN1
TP53 IN1/INP1
U7
U8
U9
U10
U11
U12
U13
U14
U15
U16
U17
X3
T1
T2
T4
T5
D1
D2
D3
SW1
STO/RDY
VDD
GND